A

MAJOR PROJECT REPORT ON

# BIO METRIC BASED VOTING MACHINE USING VERILOG

Submitted in partial fulfilment of the requirement for the award of degree of

BACHELOR OF TECHNOLOGY

IN

## ELECTRONICS AND COMMUNICATION ENGINEERING


SUBMITTED BY

| | |
|---|---|
| **JONNADA ABHISHAY RAJU** | **218R1A0488** |
| **KANNA GOPI KRISHNA** | **218R1A0489** |
| **KAMBHAMPATI VISHNU** | **218R1A0490** |
| **KANDALOJU PRASHANTH KUMAR** | **218R1A0491** |

Under the Esteemed Guidance of

**Mrs. M. Prathima**

**Assistant Professor, ECE Department**




**DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING**

# CMR ENGINEERING COLLEGE

**UGC AUTONOMOUS**

**(Approved by AICTE, Affiliated to JNTU Hyderabad, Accredited by NBA & NAAC)**

**Kandlakoya (V), Medchal (M), Telangana – 501401**


**(2024-2025)**

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## CERTIFICATE

This is to certify that the Major Project work entitled **"BIO METRIC BASED VOTING MACHINE USING VERILOG"** is being submitted by **J. ABHISHAY RAJU** bearing Roll No: **218R1A0488, K. GOPI KRISHNA** bearing Roll No: **218R1A0489 K. VISHNU** bearing Roll No: **218R1A0490, K. PRASHANTH KUMAR** bearing Roll No: **218R1A0491** in B-Tech IV-II semester, Electronics and Communication Engineering is a record Bonafide work carried out by then during the academic year 2024-25. The results embodied in this report have not been submitted to any other University for the award of any degree.

**INTERNAL GUIDE:**
Mrs. M. PRATHIMA
Assistant Professor

**HEAD OF THE DEPARTMENT:**
Dr. SUMAN MISHRA
Professor

**EXTERNAL EXAMINER**

# ACKNOWLEDGEMENTS

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# DECLARATION

We hereby declare that the project work entitled **"BIO METRIC BASED VOTING MACHINE USING VERILOG"** is the work done by us in campus at **CMR ENGINEERING COLLEGE,** Kandlakoya during the academic year 2024-2025 and is submitted as Major project in partial fulfilment of the requirements for the award of degree of **BACHELOR OF TECHNOLOGY** in **ELECTRONICS AND COMMUNICATION ENGINEERIN FROM JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD.**

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| **JONNADA ABHISHAY RAJU** | **(218R1A0488)** |
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| **KAMBHAMPATI VISHNU** | **(218R1A0490)** |
| **KANDALOJU PRASHANTH KUMAR** | **(218R1A0491)** |

# ABSTRACT

In place of the ballot papers and boxes that were formerly used in traditional voting methods, votes are now recorded using a straightforward electronic device called an electronic voting machine (EVM). The capacity to vote, or simply the right to cast a ballot, is the cornerstone of democracy. In the past, whether it was a state or centre-level election, a voter would stamp the name of their favourite candidate, fold the ballot paper following the instructions, and then deposit it in the ballot box. This is a time-consuming, difficult process that is prone to mistakes. Until automated voting machines dramatically changed the election landscape, this setup was in place. Nowadays, ballot paper, ballot boxes, stamps, etc. are replaced by a simple box known as the ballot unit of voting machines.

Since they are more difficult to lose, falsify, or trade than traditional tokens or knowledge-based IDs, biometric identifiers are regarded as more reliable for recognizing individuals. So, the most modern technology, especially the biometric system, has to be used to improve the electronic voting system. The proposed work on digital voting equipment makes it possible to conduct elections in a timely, secure, and effective manner. An algorithm, a flowchart, and the code required to put the logic into action and activate it where all created as part of the design process for this device. The suggested digital DEVM was created on Xilinx Vivado 2018.3v using Verilog HDL, and it may be used in real-time applications on an FPGA board. This article provides a comprehensive examination of voting methods, issues, and contrasts between biometric DEVMs and other voting procedures.

# CONTENTS

# LIST OF FIGURES FIGURE NO

# CHAPTER-1

# Introduction to VLSI

## 1.1 VLSI Technology

VLSI Design presents state-of-the-art papers in VLSI design, computer-aided design, design analysis, design implementation, simulation and testing. Its scope also includes papers that address technical trends, pressing issues, and educational aspects in VLSI Design. The Journal provides a dynamic high-quality international forum for original papers and tutorials by academic, industrial, and other scholarly contributors in VLSI Design.

The development of microelectronics spans a time which is even lesser than the average life expectancy of a human, and yet it has seen as many as four generations. Early 60's saw the low-density fabrication processes classified under Small Scale Integration (SSI) in which transistor count was limited to about 10. This rapidly gave way to Medium Scale Integration in the late 60's when around 100 transistors could be placed on a single chip.

It was the time when the cost of research began to decline and private firms started entering the competition in contrast to the earlier years where the main burden was borne by the military. Transistor-Transistor logic (TTL) offering higher integration densities outlasted other IC families like ECL and became the basis of the first integrated circuit revolution. It was the production of this family that gave impetus to semiconductor giants like Texas Instruments, Fairchild and National Semiconductors. Early seventies marked the growth of transistor count to about 1000 per chip called the Large-Scale Integration.

By mid-eighties, the transistor count on a single chip had already exceeded 1000 and hence came the age of Very Large-Scale Integration or VLSI. Though many improvements have been made and the transistor count is still rising, further names of generations like ULSI are generally avoided. It was during this time when TTL lost the battle to MOS family owing to the same problems that had pushed vacuum tubes into negligence, power dissipation and the limit it imposed on the number of gates that could be placed on a single die.

The second age of Integrated Circuits revolution started with the introduction of the first microprocessor, the 4004 by Intel in 1972 and the 8080 in 1974. Today many companies like Texas Instruments, Infineon, Alliance Semiconductors, Cadence, Synopsys, Celox Networks, Cisco, Micron Tech, National Semiconductors, ST Microelectronics, Qualcomm, Lucent, Mentor Graphics, Analog Devices, Intel, Philips, Motorola and many other firms have been established and are dedicated to the various fields in "VLSI" like Programmable Logic Devices, Hardware Descriptive Languages, Design tools, Embedded Systems etc.

In 1980s, hold-over from outdated taxonomy for integration levels. Obviously, influenced from frequency bands, i.e., HF, VHF, and UHF. Sources disagree on what is measured (gates or transistors)

SSI – Small-Scale Integration (0-102)
MSI – Medium-Scale Integration (102 -103)
LSI – Large-Scale Integration (103 -105)
VLSI – Very Large-Scale Integration (105 - 107)
ULSI – Ultra Large-Scale Integration (>= 107)

VLSI Technology, Inc. was a company which designed and manufactured custom and semi-custom ICs. The company was based in Silicon Valley, with headquarters at 1109 McKay Drive in San Jose, California. Along with LSI Logic, VLSI Technology defined the leading edge of the application-specific integrated circuit (ASIC) business, which accelerated the push of powerful embedded systems into affordable products. The company was founded in 1979 by a trio from Fairchild Semiconductor by way of Synertek - Jack Balletto, Dan Floyd, and Gunnar Wetlesen - and by Doug Fairbairn of Xerox PARC and Lambda (later VLSI Design) magazine.

Alfred J. Stein became the CEO of the company in 1982. Subsequently VLSI built its first fab in San Jose; eventually a second fab was built in San Antonio, Texas. VLSI had its initial public offering in 1983, and was listed on the stock market as (NASDAQ: VLSI). The company was later acquired by Philips and survives to this day as part of NXP Semiconductors.

The first semiconductor chips held two transistors each. Subsequent advances added more and more transistors, and, as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held only a few devices, perhaps as many

as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device.

Now, known retrospectively as small-scale integration (SSI), improvements in technique led to devices with hundreds of logic gates, known as medium-scale integration (MSI). Further improvements led to large-scale integration (LSI), i.e. systems with at least a thousand logic gates. Current technology has moved far past this mark and today's microprocessors have many millions of gates and billions of individual transistors.

At one time, there was an effort to name and calibrate various levels of large-scale integration above VLSI. Terms like ultra-large-scale integration (ULSI) were used. But the huge number of gates and transistors available on common devices has rendered such fine distinctions moot. Terms suggesting greater than VLSI levels of integration are no longer in widespread use.

As of early 2008, billion-transistor processors are commercially available. This is expected to become more commonplace as semiconductor fabrication moves from the current generation of 65 nm processes to the next 45 nm generations (while experiencing new challenges such as increased variation across process corners). A notable example is NVidia’s 280 series GPU. This GPU is unique in the fact that almost all of its 1.4 billion transistors are used for logic, in contrast to the Itanium, whose large transistor count is largely due to its 24 MB L3 cache. Current designs, as opposed to the earliest devices, use extensive design automation and automated logic synthesis to lay out the transistors, enabling higher levels of complexity in the resulting logic functionality.

Certain high-performance logic blocks like the SRAM (Static Random Access Memory) cell, however, are still designed by hand to ensure the highest efficiency (sometimes by bending or breaking established design rules to obtain the last bit of performance by trading stability) [citation needed]. VLSI technology is moving towards radical level miniaturization with introduction of NEMS technology. A lot of problems need to be sorted out before the transition is actually made.

## 1.2 Why VLSI?

Integration improves the design, lowers the parasitic, which means higher speed and lower power consumption and physically smaller. The Integration reduces manufacturing cost - (almost) no manual assembly.

The course will cover basic theory and techniques of digital VLSI design in CMOS technology. Topics include: CMOS devices and circuits, fabrication processes, static and dynamic logic structures, chip layout, simulation and testing, low power techniques, design tools and methodologies, VLSI architecture. We use full-custom techniques to design basic cells and regular structures such as data-path and memory.

There is an emphasis on modern design issues in interconnect and clocking. We will also use several case-studies to explore recent real-world VLSI designs (e.g. Pentium, Alpha, PowerPC Strong ARM, etc.) and papers from the recent research literature. On-campus students will design small test circuits using various CAD tools. Circuits will be verified and analyzed for performance with various simulators. Some final project designs will be fabricated and returned to students the following semester for testing.

Very-large-scale integration (VLSI) is the process of creating integrated circuits by combining thousands of transistor-based circuits into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. The term is no longer as common as it once was, as chips have increased in complexity into the hundreds of millions of transistors.

The first semiconductor chips held one transistor each. Subsequent advances added more and more transistors, and, as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device.

Now known retrospectively as "small-scale integration" (SSI), improvements in technique led to devices with hundreds of logic gates, known as large-scale integration (LSI), i.e. systems with at least a thousand logic gates. Current technology has moved far past this mark and today's microprocessors have many millions of gates and hundreds of millions of individual transistors.

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This microprocessor is unique in the fact that its 1.4 billion transistor count, capable of a teraflop of performance, is almost entirely dedicated to logic (Itanium's transistor count is largely due to the 24MB L3 cache). Current designs, as opposed to the earliest devices, use extensive design automation and automated logic synthesis to lay out the transistors, enabling higher levels of complexity in the resulting logic functionality. Certain high performance logic blocks like the SRAM cell, however, are still designed by hand to ensure the highest efficiency (sometimes by bending or breaking established design rules to obtain the last bit of performance by trading stability).

Original business plan was to be a contract wafer fabrication company, but the venture investors wanted the company to develop IC (Integrated Circuit) design tools to help fill the foundry. Thanks to its Caltech and UC Berkeley students, VLSI was an important pioneer in the electronic design automation industry. It offered a sophisticated package of tools, originally based on the 'lambda-based' design style advocated by Carver Mead and Lynn Conway. VLSI became an early vendor of standard cell (cell-based technology) to the merchant market in the early 80s where the other ASIC-focused company, LSI Logic, was a leader in gate arrays. Prior to VLSI's cell-based offering, the technology had been primarily available only within large vertically integrated companies with semiconductor units such as AT&T and IBM.

VLSI's design tools eventually included not only design entry and simulation but eventually cell-based routing (chip compiler), a data path compiler, SRAM and ROM compilers and a state machine compiler. The tools were an integrated design solution for IC design and not just point tools, or more general-purpose system tools. A designer could edit transistor-level polygons and/or logic schematics, then run DRC and LVS, extract parasites from the layout and run Spice simulation, then back-annotate the timing or gate size changes into the logic schematic database. Characterization tools were integrated to generate Frame Maker Data Sheets for Libraries. VLSI eventually spun off the CAD and Library operation into Compass Design Automation but it never reached IPO before it was purchased by Avanti Corp.

VLSI's physical design tools were critical not only to its ASIC business, but also in setting the bar for the commercial EDA industry. When VLSI and its main ASIC competitor, LSI Logic, were establishing the ASIC industry, commercially-available tools could not deliver the productivity necessary to support the physical design of hundreds of ASIC designs each year without the deployment of a substantial number of layout engineers.

Companie’s development of automated layout tools was a rational "make because there's nothing to buy" decision. The EDA industry finally caught up in the late 1980s when Tangent Systems released its Tan Cell and Tan Gate products. In 1989, Tangent was acquired by Cadence Design Systems (founded in 1988).

Unfortunately, for all VLSI's initial competence in design tools, they were not leaders in semiconductor manufacturing technology. VLSI had not been timely in developing a 1.0 µm manufacturing process as the rest of the industry moved to that geometry in the late 80s. VLSI entered a long-term technology partnership with Hitachi and finally released a 1.0 µm process and cell library (actually more of a 1.2 µm library with a 1.0 µm gate).

As VLSI struggled to gain parity with the rest of the industry in semiconductor technology, the design flow was moving rapidly to a Verilog HDL and synthesis flow. Cadence acquired Gateway, the leader in Verilog hardware design language (HDL) and Synopsys was dominating the exploding field of design synthesis. As VLSI's tools were being eclipsed, VLSI waited too long to open the tools up to other fabrications and Compass Design Automation was never a viable competitor to industry leaders.

Meanwhile, VLSI entered the merchant high speed static RAM (SRAM) market as they needed a product to drive the semiconductor process technology development. All the large semiconductor companies built high speed SRAMs with cost structures VLSI could never match. VLSI withdrew once it was clear that the Hitachi process technology partnership was working.

ARM Ltd was formed in 1990 as a semiconductor intellectual property licensor, backed by Acorn, Apple and VLSI. VLSI became a licensee of the powerful ARM processor and ARM finally funded processor tools. Initial adoption of the ARM processor was slow. Few applications could justify the overhead of an embedded 32bit processor. In fact, despite the addition of further licensees, the ARM processor enjoyed little market success until they developed the novel 'thumb' extensions. Ericsson adopted the ARM processor in a VLSI chipset for its GSM handset designs in the early 1990s. It was the GSM boost that is the foundation of ARM the company/technology that it is today.

Only in PC chipsets, did VLSI dominate in the early 90s. This product was developed by five engineers using the 'Mega cells" in the VLSI library that led to a business unit at VLSI that almost equaled its ASIC business in revenue. VLSI eventually ceded the market to Intel because Intel was able to package-sell its processors, chipsets, and even board level products together.

VLSI also had an early partnership with PMC, a design group that had been nurtured of British Columbia Bell. When PMC wanted to divest its semiconductor intellectual property venture, VLSI's bid was beaten by a creative deal by Sierra Semiconductor. The telecom business unit management at VLSI opted to go it alone. PMC Sierra became one of the most important telecoms ASSP vendors.

Scientists and innovations from the 'design technology' part of VLSI found their way to Cadence Design Systems (by way of Redwood Design Automation). Compass Design Automation (VLSI's CAD and Library spin-off) was sold to Avant! Corporation, which itself was acquired by Synopsys.

## 1.3 Structured Design

Structured VLSI design is a modular methodology originated by Carver Mead and Lynn Conway for saving microchip area by minimizing the interconnect fabrics area. This is

obtained by repetitive arrangement of rectangular macro blocks which can be interconnected using wiring by abutment. An example is partitioning the layout of an adder into a row of equal bit slices cells. In complex designs this structuring may be achieved by hierarchical nesting.

Structured VLSI design had been popular in the early 1980s, but lost its popularity later because of the advent of placement and routing tools wasting a lot of area by routing, which is tolerated because of the progress of Moore's Law. When introducing the hardware description language KARL in the mid' 1970s, Reiner Hartenstein coined the term "structured VLSI design" (originally as "structured LSI design"), echoing Edger Dijkstra's structured programming approach by procedure nesting to avoid chaotic spaghetti structured programs.

## 1.4 Applications of VLSI

- Electronic system in cars.
- Digital electronics control VCRs
- Transaction processing system, ATM
- Personal computers and Workstations
- Medical electronic systems.

Electronic systems now perform a wide variety of tasks in daily life. Electronic systems in some cases have replaced mechanisms that operated mechanically, hydraulically, or by other means; electronics are usually smaller, more flexible, and easier to service. In other cases, electronic systems have created totally new applications. Electronic systems perform a variety of tasks; some of them are visible while some are hidden.

Personal entertainment systems such as portable MP3 players and DVD players perform sophisticated algorithms with remarkably little energy. Electronic systems in cars operate stereo systems and displays; they also control fuel injection systems, adjust suspensions to varying terrain, and perform the control functions required for anti-lock braking systems.

Digital electronics compress and decompress video, even at high-definition data rates, on the-fly in consumer electronics. Low-cost terminals for Web browsing still require sophisticated electronics, despite their dedicated function. Personal computers and

workstations provide word-processing, financial analysis, and games. Computers include both central processing units and special-purpose hardware for disk access, faster screen display, etc. Medical electronic systems measure bodily functions and perform complex processing algorithms to warn about unusual conditions. The availability of these complex systems, far from overwhelming consumers, only creates demand for even more complex systems.

The growing sophistication of applications continually pushes the design and manufacturing of integrated circuits and electronic systems to new levels of complexity. And perhaps the most amazing characteristic of this collection of systems is its variety-as systems become more complex, we build not a few general-purpose computers but an ever-wider range of special-purpose systems. Our ability to do so is a testament to our growing mastery of both integrated circuit manufacturing and design, but the increasing demands of customers continue to test the limits of design and manufacturing.

## 1.5 ASIC

An Application-Specific Integrated Circuit (ASIC) is an integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use. For example, a chip designed solely to run a cell phone is an ASIC. Intermediate between ASICs and industry standard integrated circuits, like the 7400 or the 4000 series, are application specific standard products (ASSPs).

As feature sizes have shrunk and design tools improved over the years, the maximum complexity (and hence functionality) possible in an ASIC has grown from 5,000 gates to over 100 million. Modern ASICs often include entire 32-bit processors, memory blocks including ROM, RAM, EEPROM, Flash and other large building blocks. Such an ASIC is often termed a SoC (system-on-a-chip). Designers of digital ASICs use a hardware description language (HDL), such as Verilog or VHDL, to describe the functionality of ASICs.

Field-programmable gate arrays (FPGA) are the modern-day technology for building a breadboard or prototype from standard parts; programmable logic blocks and programmable interconnects allow the same FPGA to be used in many different applications. For smaller designs and/or lower production volumes, FPGAs may be more cost effective than an ASIC design even in production.

- An application-specific integrated circuit (ASIC) is an integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use.
- A Structured ASIC falls between an FPGA and a Standard Cell-based ASIC
- Structured ASICs are used mainly for mid-volume level designs
- The design task for structured ASIC's is to map the circuit into a fixed arrangement of known cells

## 1.6 ASIC Design Flow

As with any other technical activity, development of an ASIC starts with an idea and takes tangible shape through the stages of development as shown in Fig 1 and in Fig 2. The first step in this process is to expand the idea in terms of behaviour of the target circuit.

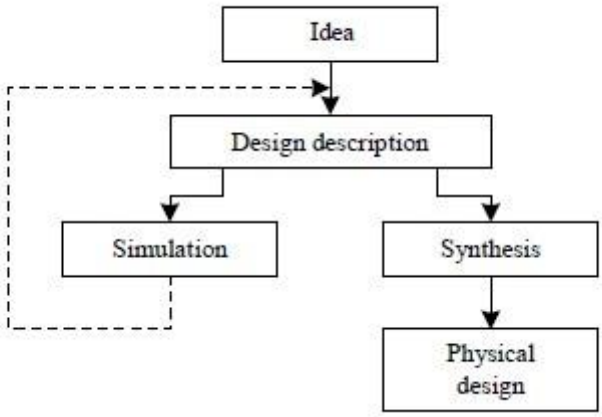


**FIGURE 1: DEVELOPMENT OF ASIC**

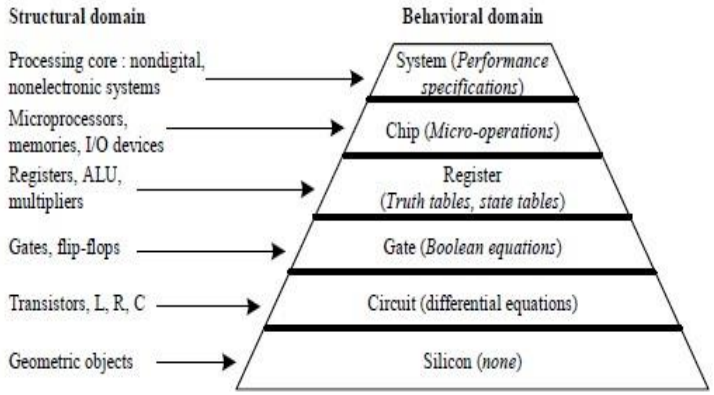


**FIGURE 2: ASIC DESIGN FLOW**

The design is tested through a simulation process; it is to check, verify, and ensure that what is wanted is what is described. Simulation is carried out through dedicated tools. With every simulation run, the simulation results are studied to identify errors in the design description. The errors are corrected and another simulation run carried out. Simulation and changes to design description together form a cyclic iterative process, repeated until an error-free design is evolved.

Design description is an activity independent of the target technology or manufacturer. It results in a description of the digital circuit. To translate it into a tangible circuit, one goes through the physical design process. The same constitutes a set of activities closely linked to the manufacturer and the target technology.

## 1.7 Very Large-Scale Integrated circuitry

Very large-scale integrated circuitry is playing a key role in the development of modern electronic systems at APL. In the Microelectronics Group, activities have been focused on creating a resource to ensure that all personnel have access to high-performance, high reliability integrated circuits. This article describes progress in the design, acquisition, packaging, testing, and insertion of very large-scale integrated circuits. INTRODUCTION The fabrication of integrated circuits has progressed to the point where a million transistors can be placed on a single piece of silicon about one-quarter the size of a U.S. dime. Such a "chip" or integrated circuit is shown in Chips possessing that level of complexity are generally classified as very large scale integrated (VLSI) circuits. VLSI chips are being produced by major semiconductor manufacturers primarily for the computer, automobile, and home entertainment markets. Typical chips in production include 32-bit microprocessors and large, 256-kilobit (and even I-megabit) random access memories. With most manufacturers of semiconductor devices directing their products toward the mass markets, the military, which by integrated circuit industry standards uses very few chips, found itself without sources of VLSI circuitry to meet its stringent future performance needs. The military requires fast chips (up to 10 14 gate-hertz per square centimetre I) that are extremely reliable and can survive the rigors of a broad spectrum of applications environments.

To create and acquire suitable high-performance VLSI-like integrated circuits, the Department of Défense established 2 in 1978 its own VLSI program, called the Very Highspeed Integrated Circuit (VHSIC) Program. Both commercial VLSI manufacturers and

the VHSIC program are now producing individual devices, circuits, and families of multiple chips suitable for use in future military systems. It is quite clear that high-performance systems must contain the latest, fastest, and most flexible VLSII VHSIC chips available. APL, in its role as a prime developer of advanced prototype electronic systems for use in space, under water, in avionics, and for Fleet defences, needs access to these VLSI/VHSIC devices. Consequently, several years ago, APL created a VLSI task team. Based on the team's findings and the growing impact of VLSI worldwide, VLSI was made both an important part of Independent Research and Development efforts and a focused development activity in the Microelectronics Group. It is the mission of the VLSI effort to ensure access to high-performance, high-reliability integrated circuits.

Johns Hopkins A PL Technical Digest, Volume 7, Number 3 (1986) ed after Integrate circuit (gate a ray). Integrated circuit (gate array), chip or die Enlarged die. showing metallization detail Figure 1-lntegrated circuit chip. Progress has been made in several areas, including design, acquisition (fabrication), packaging, testing, and system insertion. The interrelation of these activities in the development sequence for an application-specific integrated circuit (ASIC) is shown in the coloured lines represent optional hand-off points between in-house development and outside vendor development or ser271 Charles, Boland, Wagner - Very Large-Scale Integrated Circuitry Design Fabrication Test

Packaging Test Insertion Design Specification In-house Development Design Capture Semiconductor vendor development/services. Flow diagram for the development of an ASIC. vices. The chip development and insertion process involve not only the expenditure of significant resources, but also the need to make several decisions concerning internal versus external activities, especially in the area of acquisition. ASICs are available in several different forms, including full-custom, standard cell, gate-array, and linear array circuits. The principal difference among the forms is the degree of customization of the layout of transistors that implement the desired circuit. The transistor layouts and interconnections for full-custom and standard cell circuits are unique.

Gate arrays (digital) and linear arrays (analog) have regular arrays of rediffused transistors whose interconnection can be customized to implement different circuits simply by patterning one or two metallization levels. The patterning is performed in a manner analogous to patterning a printed wire board on a hybrid substrate4 and thus represents a natural extension of APL's photolithographic technology. DESIGN APL's custom or

application-specific design and development capabilities (from gate arrays to full-custom circuits) are based on the Mentor computer-aided engineering workstation, a powerful single-user system that provides a generic set of tools for all design tasks.

The Circuit schematic Functional cell library Physical cell library Functionally design database Back annotation Physical design database Test vector file Pattern generation tape Figure 3-Flow diagram of a typical ASIC design. Mentor software has been augmented with different library file sets specific to various vendor's ASIC structures. shows a flow diagram of a typical application-specific chip design process.

The process begins with the entry of a logic schematic (circuit design at the logic-gate level) into the Mentor system using its graphical input and editing tools. The schematic may begin as a high-level functional block diagram that is successively refined until the design is drawn entirely with recharacterized logic macros or cells that include the common functions used by logic designers. The functional cell library contains symbols·, behavioural models, and the performance characteristics for each cell.

The library data are combined with the cell-incidence and connectivity data from the schematic to create a functional design database that serves as the input to the simulation and layout operations. In the next step behaviour and performance data for all cells in the design are combined to simulate the function and timing for the entire design. Using the Mentor interactive logic simulator, test inputs are applied to the circuit model, and outputs are calculated and displayed for analysis by the designer.

Internal circuit nodes can be easily "probed" during simulation by· simply pointing to them in the schematic. Timing waveforms are calculated using typical values for cell propagation delays and estimates for interconnection path delays. (Accurate values for interconnection delays are calculated during the back-annotation step described below.) On the basis of simulation results, changes to the design may be required as indicated by the dashed line in Design and simulation is an iterative. process that continues Johns Hopkins APL Technical Digest, Volume 7, Number 3 (/986) until the simulation results satisfy all functional and performance specifications. Once the design has been verified through simulation, the physical layout of the circuit consisting of two parts, cell placement and the routing of cell interconnections, can be done (step 3).

The tasks are guided and constrained by design rules contained in the physical library, which also contains either a transistor interconnection pattern for each cell (for array structures) or a complete set of masking-level patterns to fabricate each cell from scratch (for standard cell and full-custom approaches). After physical layout, accurate signal interconnection delays can be calculated from the actual path lengths recorded in the physical design database.

The delay values are used to update the timing estimates in the functional design database so that a more accurate simulation can be performed. The process, called back-annotation (step 4), will help designers identify timing problems and may dictate further changes to the schematic or layout. A pattern generation program (step 5) is used to write (on tape) the top-level metal interconnection pattern for gate arrays or the multiple mask-level patterns for standard cell or full-custom designs. The pattern tape is used by the semiconductor fabrication house or a foundry to produce the optical masks required for wafer processing. (A wafer is a th11l slice of semiconductor material on which hundreds of chips are fabricated.)

The final step in the design process (step 6) involves extracting test inputs from a log produced by the software simulation of the design to produce a test vector file for wafer and packaged part testing. The file can be transferred electronically to the test equipment as required. ACQUISITION As shown in Fig. 2, acquisition of the custom VLSI circuits can follow several routes, depending on factors such as circuit type and complexity, inhouse capabilities, and cost. In most custom VLSI (full-custom and standard cell) design methodologies, fabrication cannot begin until the circuit design and layout have been completed because the size and placement of transistors on the chip are different for each design.

However, gate arrays allow most of the semiconductor processing steps to proceed independently of the design process because the size and placement of transistors are fixed. Processing of a gate-array integrated circuit comprised of arrays of standard transistors or logic gates with interconnection space is partially completed by a silicon foundry. The interconnections of those transistors or gates to implement the desired circuit function are made later. The partially completed circuits are called "uncommitted gate arrays" because all the active devices (transistors and gates) have been fabricated but they have not been interconnected for a specific application.

The gate array circuits are fabricated on wafers and then stockpiled until the interconnections of transistors or gates have been defined. In order to complete the circuit or customize it, the desired pattern of interconnections is derived from a circuit design and then etched on the surface of the wafer by a photolithographic process. Johns Hopkins APL Technical Digest, Volume 7, Number J (1986) Charles, Boland, Wagner - Very Large-Scale Integrated Circuitry The major advantages of gate arrays when compared to other custom VLSI design alternatives are faster turnaround of designs, lower cost for small quantities higher designer productivity (transistors per manhour),6 and most mature ASIC technology. As in all engineering, some compromises are made in order to gain these advantages.

Hence, some of the limitations of gate arrays are their less-than-optimum circuit density, power consumption, and speed performance, and their greater cost for large quantities (more than 10,000 to 100,000 devices). In 1976, APL began using gate arrays in a variety of designs. Since then, more than 10 different designs have been created, nearly all in complementary metal oxide semiconductor (CMOS) technology, but there was at least one in high-speed bipolar technology. The gate arrays have been used primarily for biomedical and space applications that require low power and small size, and the number of logic gates in these arrays has varied from 250 to 1000. Since each gate array replaces many standard integrated circuits, system reliability has been improved. While APL's experience with developing functional gate arrays has been good, dealing with the semiconductor manufacturers for small quantities has not been as successful. Generally, APL has been restricted to working with smaller companies and has not been assured of getting the best response on service for small tasks. Other laboratories with similar goals have noted the same problems and concerns. A few, including the Lawrence Livermore Laboratory 7 and the Ft. Monmouth Army Laboratory, have developed internal capabilities for patterning their own gate arrays.

It is for these reasons that APL has established an in-house gate-array development service. The wafer processing step in fabrication, shown on the left side of Fig. 2, involves purchasing uncommitted gate-array wafers from outside suppliers. The capital investment required to produce them in-house is not justified because of our very low production requirements. However, it is reasonable to customize the wafers here because most of the facilities are already in place in the Microelectronics Laboratory for hybrid circuit development.

The selection of a gate array and a supplier was guided by several factors: anticipated circuit size and performance requirements, existing processing capabilities, existing computer-aided engineering facilities, past experience with commercial gate-array products and services, and cost. A thorough evaluation of commercially available gatearray wafers 8 led to the selection of the GA-2500 gate array from Gould Semiconductors. The array is fabricated by means of a 3-micrometer CMOS technology that offers many desirable characteristics: low power consumption, high noise immunity, high performance, and high density.

The array contains over 10,000 transistors (or the equivalent of 2500 2-input NAND gates) and 84 pads for input and output signals. One level of metallization is used on the array for transistor interconnections. 273 Charles, Boland, Wagner - Very Large-Scale Integrated Circuitry As our experience with the gate array develops, other arrays (both digital and analog) will be added to the list of those available in-house.

A high-priority new array will be one that has significant radiation hardness~ Another array will extend the processing capability to double-level metal (where two levels of metal are used on the array for interconnection), thus allowing uses of larger and higher performance arrays to meet future needs. Design and engineering support for the acquisition of custom chips and arrays (which do not fall into the range of the current internally available gate arrays) will be readily available from the Microelectronics Group. PACKAGING Packaging-the science and art of providing electrical interconnections, thermal management, mechanical support, and environmental protection for integrated circuits-it is an extremely important activity in the VLSII VHSIC arena.

High-performance integrated circuit chips must have well-designed packaging to ensure that their performance integrity will be maintained when they are inserted into the system. Poor packaging can significantly slow a high-speed chip or can prevent it from functioning. The VLSIIVHSIC era puts special demands on packaging, including low inductance and -capacitance interconnections for high-speed operation, packaging materials having matched temperature coefficients of expansion and high thermal conductivity to handle the increased chip power densities that result from device scaling and configurations that can support input! output requirements ranging to 300 leads and beyond. Such demands cannot be satisfied by today's dominant packaging technology: the dual in-line package.

Dual in-line packages are basically limited to 64 leads (on 100-mil Package type Pin pitch (mils) centres down two long sides of a rectangular package structure) because of their poor input! Output count-to area ratio. Sixty-four-lead dual in-line packages are typically several inches long and 1 inch wide and weigh approximately 12 ounces in the ceramic form. Fortunately for VLSIIVHSIC, there is at least one high-density packaging option, the ceramic chip carrier, that promises to satisfy the stringent demands of the new technologies. Figure 4 compares various package input! output capabilities with major device and system input! output requirements.

Chip carriers offer high-density input! output performance while providing reduced size and weight and improved electrical parameters over the dual in-line package. They are designed for surface mounting, which involves mounting the leadless (or, in some cases, leaded) components directly to the top surface of a circuit board. In contrast, the dual inline package leads must be soldered into predrilled and plated holes; this technique is known as through-hole mounting. As shown in Fig. 4, the pin grid array is a high-density packaging alternative for through-hole mounting. In through-hole mounting packages that have bottom leads such as pin grid arrays, the leads are soldered into plated through holes (vias) in multiple-layer printed wire boards. The holes are typically placed on 100-rnil centres (100-mil grid). In addition to holding the component lead, they serve as a via for interconnection between circuit board layers.

This type of mounting has several disadvantages for VLSI and VHSIC applications, including reduced board density (due to via structure), difficulty to repair (as input! output numbers increase), and increased inductance due to round wire leads. The repair or removal of this type of package can be facilitated by the use of a socket that is permanently mounted into the board. The package can then be plugged into and Input/output count or application 100150 r 40125120 j,2.511f5 20 60 100 140 180 220 260 300 Dual in-line Standard High density Pin grid array Standard High density Chip carriers Standard (Idealess) High density (Idealess) Standard (leaded) High density (leaded) Applications Single-device family Memory (multichip) Microprocessor (multi-chip) Light emitting diode driver. Gate array/custom.

Package and application input/output capability and requirements. 274 Johns Hopkins APL Technical Digest, Volume 7, Number 3 (1986) out of the socket. However, sockets add additional inductance and resistance to the circuit path that can degrade device

performance. Mechanical integrity would also be questionable for high-reliability applications. The Group has geared its VLSI/VHSIC packaging technology toward surface mounting with ceramic chip carriers on multilayer ceramic boards to affect the best possible temperature coefficient of expansion match. A description of the Microelectronics Laboratory's multilevel thick-film ceramic board technology is given in an article by Romenesko et ale elsewhere in this issue.

To verify that the ceramic chip carrier provides a viable high-performance package for APL's custom chip first level packaging requirements, comprehensive electrical, thermal, and mechanical modelling activities have been undertaken. The models, based on finite element modelling techniques, have been validated by controlled experimentation and have already been used to develop design guidelines for dense circuit applications such as , the digital signal processor in the Naval Remote Ocean Sensing System program. A detailed description of the methodology for thermal and thermomechanical modelling is given in an article by Clatterbaugh and Charles elsewhere in this issue.

The article also presents various validation experiments that show that the ceramic chip carrier/ceramic board system can be reliable under extreme environmental conditions such as temperature cycling (- 55 to + 125°C) and power cycling. 10 Finite-element modelling has been used to numerically estimate the capacitance, inductance, and characteristic impedance of serial lines in multiconductor environments typical of high-speed digital signal-processing applications that are representative of VHSIC brass board systems.

If a bipolar logic family were selected, for example, a design concern might be the characteristically low impedance (8 to 20 ohms) of a standard thick-film multilayer circuit. Low-impedance lines that connect bipolar logic forms can cause significant propagation delays for logically-to-O transitions and, to a lesser extent, for logical O-to-l transitions with an undetermined amount of loss in noise margin. The problem worsens with increasing line length. Finite-element modelling techniques can be used to develop design guidelines for increasing the characteristic impedance and hence for improving the performance of this bipolar logic family, especially at high frequencies.

Design guidelines are focused on reducing the overall capacitance of critical signal lines, on providing adequate power supply decoupling of switching transients, and on

ensuring low-impedance ground returns. A typical impedance-versus-buried-Layer position TESTING We are developing a flexible test system and procedures for the automated testing of fast, complex integrated circuits.

The automated test equipment system is built around Hewlett Packard 16- and 32-bit computers driving a suite of bus programmable test equipment. A typical equipment configuration for conducting several important parametric and functional tests is shown in Johns Hopkins APL Technical Digest, Volume 7, Number 3 (/986) Charles, Boland, Wagner - Very Large-Scale Integrated Circuitry 30u. S: Ci> c. (Jl 20 "0 co '0 u: sell g 10-mile line centred over lines grid mil line centred between grid spaces, 7 .5-milline centred over grid re 10-mll Ime " /' centred. over grid 1 O-mill line spaces " Centre? over “j” grid Impey. 7.5-mile line centred over grid spaces co 10 Buried conductor levels Figure 5-Calculated Signal line capacitance and high frequency (100 megahertz) impedance for a multilayer thick film ceramic circuit board with a gridded ground plane (0.015-inch lines on 0.050-inch centre’s). A 0.001 -inch dielectric thickness between conductor levels is assumed. The level numbers indicate inverse distance from the ground plane with level 1 being the farthest removed and level 4 the closest.

The equipment can handle both packaged chips, using a socketed fixture, and unpackaged chips/wafers, using a compatible probe card or precision micromanipulator probes. One especially powerful feature of this modular type of system is its flexibility. The equipment shown can easily be reconfigured or replaced with higher performance equipment to satisfy unique or new test requirements.

The test system is programmed to apply a sequence of stimuli (test vectors) to the device under test, to sample the outputs, and to compare them to the design specifications. The test vectors can be extracted from the Mentor computer -aided engineering workstation after software simulation of the design, or they can be programmed directly at the test computer console. In the VLSIIVHSIC world, device testing (and packaging) should be an integral part of the design process. Consequently, we have emphasized a design-for testability philosophy, and we encourage all designers to include some form of on-chip testing and self-diagnosis capabilities.

Many testing operations have already been performed on VLSI/VHSIC devices, including the APL-developed APL-IA and spectrum accumulator chips, II VHSIC Static

Random-Access Memories (SRAMs), APL-developed gate arrays, and some commercial silicon and gallium arsenide parts. The system in Fig. 6 was used for most of these tests although, in a few cases, a special purpose dedicated tester was required to provide some unique function or capability. For example, two stand275alone dedicated testers were developed to test the VHSI C 72K SRAMs supplied by Texas Instruments With the two, we were able to verify the high-speed performance of the SRAM, measure the non-pipeline memory timing parameters, and display a real-time bit-error map to observe the pattern sensitivity of the chip. While the Texas Instruments SRAM was specified at 25-megahertz, actual performance at room temperature was demonstrated up to 50 megahertz (which was the limit of our tester).

A further example of VLSI testing is that recently performed on a l000-gate CMOS array developed for the Bird-Borne Tracking System. The custom gate array was designed as part of a system that would be attached to migratory birds in order to track their flight via satellite. A test program was developed to verify and mea276 IEEE 488 bus FTS PAC-7010 air jet -70 to + 150°C dry air Device specific electronics Test table Thermal test head Standard multiplex switches Custom device interface Device under test sure performance of the devices using an earlier version of the Hewlett Packard computer-based test system.

Since the effects of radiation on VLSI circuits were not well understood, special tests using the APL cobalt 60 radiation tester were performed on the bird-borne CMOS gate arrays. Using the tests developed for the Hewlett Packard system, we were able to perform functional and parametric testing of the gate-array devices promptly after subjecting them to radiation doses up to 105 rads. These particular devices performed adequately up to radiation levels of 5 x 104 rads although some performance degradation was clearly evident at those doses. Figure 7 illustrates how one of the crucial parameters, the operating current, increased as the radiation dose accumulated.

## 1.8 Technology Insertion

We have been active in the introduction of custom chip technology into several programs, including towed array chain electronics, space tracking and switching applications, and VHSIC interoperability. The towed array project involves the design of a 3500-gate CMOS array for use in the second-generation underwater data acquisition module. The gate array replaces 10 medium- and large-scale integrated circuits used in the initial design, reduces the

size and power consumption of the circuit, and permits the addition of new functional capabilities. All aspects of the development of this gate array except the integrated-circuit processing were completed in-house using the facilities and methodology described in this article. A particularly interesting interoperability project is the VHSIC Programmable Interface Adapter (VPIA). The goal of the VPIA design team is to design and simulate a preliminary interface of the Texas Instruments VHSIC bus (M bus) to the Honeywell VHSIC bus (L bus). To simplify the design effort, it was decided to implement an M bus slave to the L bus master interface. The M bus side or slave side of the VPIA looks like a peripheral to the M bus central processing unit. The L bus side (the master side) looks like a central processing unit in that it can take control of the bus and generate control and address signals. This allows direct memory access read or write transfers on the L bus side to a central processing unit or a direct memory access device on the M bus via the VPIA. A block diagram of the currently configured VPIA.

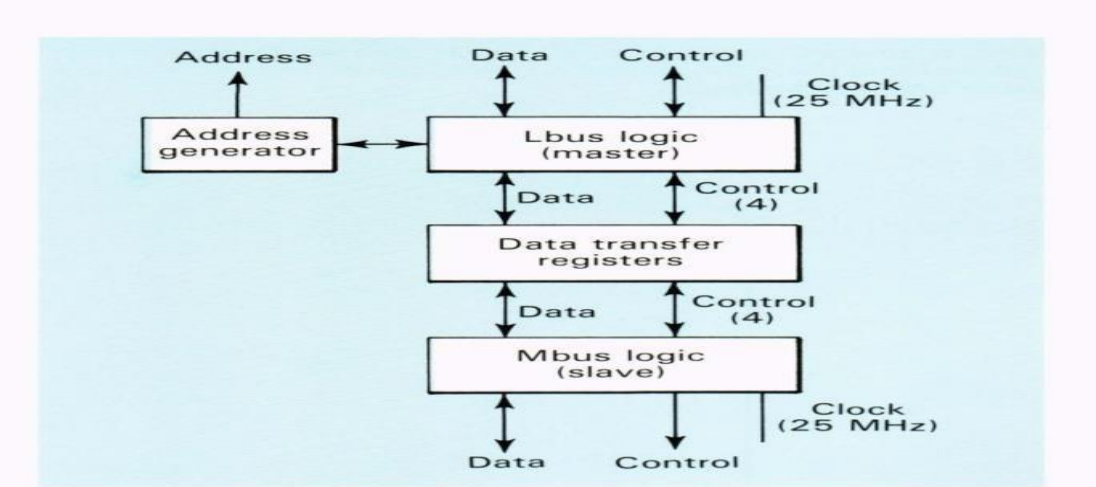


**FIGURE 3: BLOCK DIAGRAM OF THE VHSIC PROGRAMMABLE INTERFACE ADAPTER**

## 1.9 Packaging

Packaging-the science and art of providing electrical interconnections, thermal management, mechanical support, and environmental protection for integrated circuits-it is an extremely important activity in the VLSII VHSIC arena. High-performance integrated circuit chips must have well-designed packaging to ensure that their performance integrity will be maintained when they are inserted into the system. Poor packaging can significantly slow a high-speed chip or can prevent it from functioning.

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In contrast, the dual in-line package leads must be soldered into predrilled and plated holes; this technique is known as through-hole mounting. As shown in Fig. 8, the pin grid array is a high-density packaging alternative for through-hole mounting. In through-hole mounting packages that have bottom leads such as pin grid arrays, the leads are soldered into plated through holes (vias) in multiple-layer printed wire boards. This type of mounting has several disadvantages for VLSI and VHSIC applications, including reduced board density (due to via structure), difficulty to repair (as input! output numbers increase), and increased inductance due to round wire leads.

The repair or removal of this type of package can be facilitated by the use of a socket that is permanently mounted into the board. The package can then be plugged into and Input/output count or application, Dual in-line Standard High density Pin grid array Standard High density Chip carriers Standard (Idealess) High density (Idealess)Standard (leaded) High density (leaded) Applications Single-device family Memory (multichip) Microprocessor (multi-chip) Light emitting diode driver. Gate array/custom Package and application input/output capability and requirements.

# CHAPTER-2

## Introduction

In democratic countries like us the election process be the curtail for a future of respectable country. With in an election process voting of votes which represent pulse of people. The mode of vote casting is done by different methodology. Now our proposal is Xilinx based electronic voting machine. It is designed on Xilinx ISE using Verilog HDL, which is implemented on ASIC (APPLICATION SPECIFIC INTEGREATED CIRCUIT). In order to perform to perform this mechanism, there are several phases in designing flowchart, algorithm and simultaneously code is developed to simulation of logic.

### 2.1 History

Elections are conducted to elect the people's leader through the voting process. In India election are conducted by Election Commission of India. It is a one of independent central based Organization which is established in 1950.The first election of 1951-52, it was quite difficult task for Election commission by using ballet papers.

### 2.1.1 Evolution of Election Process

#### 2.1.1.1 Election Process by Using Ballot Papers

In beginning days, the votes casted based on ballot papers here each one voter individually Walk in a polling booth then the poling preceding officer check whether that person vote is Present in that polling booth or not if present then officer give a ballot paper consist candidates Who are participated in elections, then voter should choose his option then there would Specific boxes to carry the ballot slips. After that on voter's left hand little finger mark with a Inerasable ink. Poling is done across the different polling stations in constancy in given specific Time. But here lot of procedures with in it like printing a Ballot vote paper charring, providing Security Management. Here there is chance to manipulate also prone to errors.

### 2.1.1.2 Election Process by EVM

Later to overcome the in justification of paper ballots, EVMs came into existence. Supreme Court ordered to implement EVM's for election procedures in year 1982. EVM's are first used in Kerala, North Paravur constituency as a Pilot Project in 1982. Since then, EVM's are used for voting process.

#### 2.1.1.2.1 Introduction of VVPAT'S

Since utilize of EVM, the opponent contestants rises that the EVM'S are indirectly favourable to the who are in government. So, our higher authority tribunal of honourable Supreme Court questioned the EC to provide a solution for it. a long working on it the Election Commission introduce a VVPAT (VOTER-VERIFIABLE PAPER AUDIT TRAIL), which first time used in September 2013 in Noksen (assembly constituency) in Nagaland. VVPAT along with EVM used on large scale for first in India in assembly seats out of 40 in 2013 in Mizoram legislative assembly election.

# CHAPTER-3

# Existing Election Procedure

## 3.1 EVM

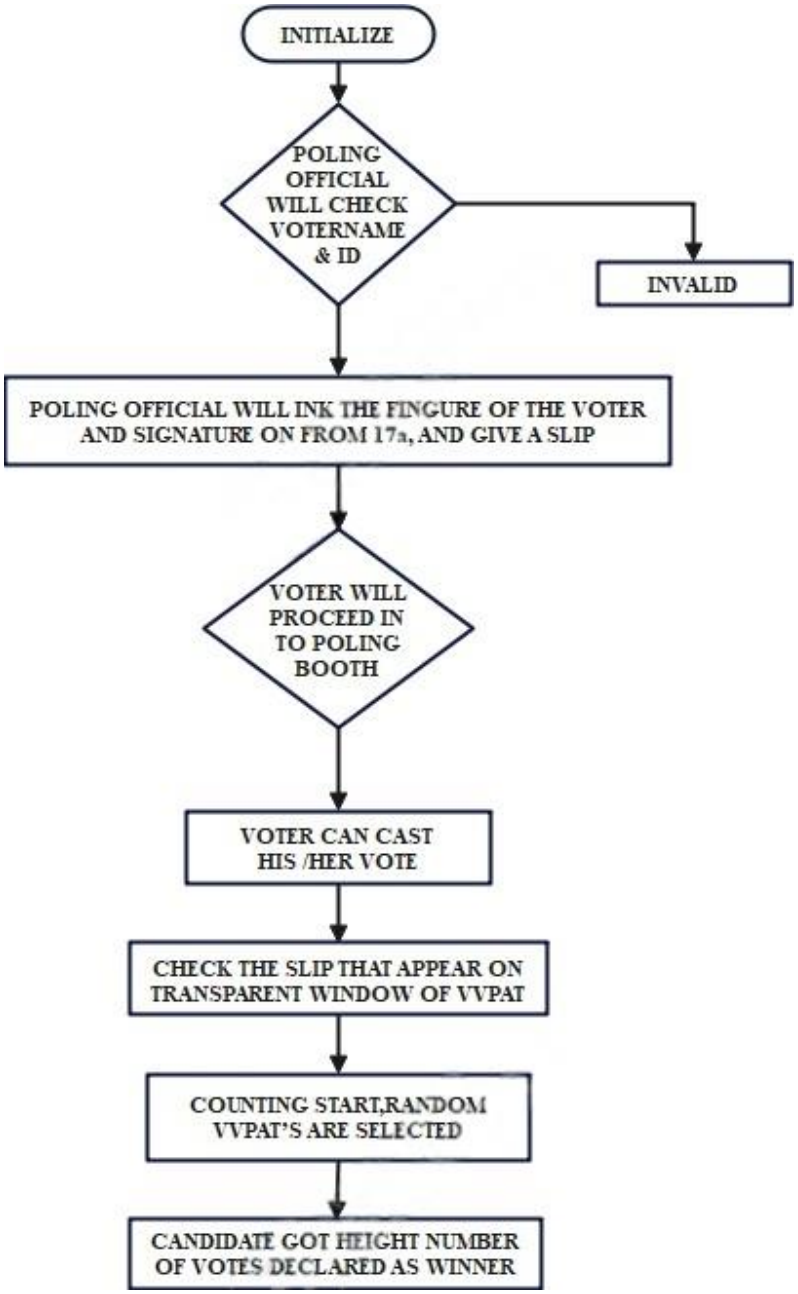


**FIGURE 4:FLOW CHART FOR EXISTING ELECTION PROCEDURE**

## 3.2 EVM

The Indian electronic voting machine (EVM) were developed in 1989 by Election Commission of India in collaboration with Bharat Electronics Limited and Electronics Corporation of India Limited. The Industrial designers of the EVMs were faculty members at the Industrial Design Centre, IIT Bombay. The EVMs were first used in 1982 in the by-election to North Paravur Assembly Constituency in Kerala for a limited number of polling stations. The EVMs were first time used on an experimental basis in selected constituencies of Rajasthan, Madhya Pradesh and Delhi. The EVMs were used first time in the general election (entire state) to the assembly of Goa in 1999. In 2003, all by-elections and state elections were held using EVMs, encouraged by this election commission decided to use only EVMs for Lok Sabha elections in 2004.

## 3.3 Design Flow


**FIGURE 5: EXISTING EVM MODAL**

**Ballot Unit (left), control unit (right)**

The EVM was designed by two professors of IIT Bombay, A.G. Rao and Ravi Poovaiah. An EVM consists of two units, a control unit, and the balloting unit. The two units are joined by a five-meter cable. Balloting unit facilitates voting by a voter via labelled buttons while the control unit controls the ballot units, stores voting counts and displays the results. The controller used in EVMs has its operating program etched permanently in silicon at the time of manufacturing by the manufacturer. No one (including the manufacturer) can change the program once the controller is manufactured. The control unit is operated by one of the polling booth officers, while the balloting unit is operated by the voter in privacy.

The officer confirms the voter's identification then electronically activates the ballot unit to accept a new vote. Once the voter enters the vote, the balloting unit displays the vote to the voter, records it in its memory. A "close" command issued from the control unit by the polling booth officer registers the vote, relocks the unit to prevent multiple votes. The process is repeated when the next voter with a new voter ID arrives before the polling booth officer.

EVMs are powered by an ordinary 6 volt alkaline battery manufactured by Bharat Electronics Limited, Bangalore and Electronics Corporation of India Limited, Hyderabad. This design enables the use of EVMs throughout the country without interruptions because several parts of India do not have the power supply and/or erratic power supply.

The two units cannot work without each other. After a poll closes on a particular election day, the units are separated and the control units moved and stored separately in locked and guarded premises both units have numerous tamper-proof protocols. Their hardware, by design, can only be programmed once at the time of their manufacture and they cannot be reprogrammed. They do not have any wireless communication components inside, nor any internet interface and related hardware.

The balloting unit has an internal real-time clock and a protocol by which it records every input-output event with a timestamp whenever they are connected to a battery pack. The designers intentionally opted for battery power, to prevent the possibility that the power cables might be used to interfere with the reliable functioning of an EVM.

An EVM can record a maximum of 3840 (now 2000) votes and can cater to a maximum of 64 candidates. There is provision for 16 candidates in a single balloting unit and up to a maximum of 4 balloting units with 64 candidate names and the respective party symbols can be connected in parallel to the control unit. If there are more than 64 candidates, the conventional ballot paper/box method of polling is deployed by the Election Commission. After a 2013 upgrade, an Indian EVM can cater to a maximum of 384 candidates plus "None of The Above" option (NOTA).

The current electronic voting machines in India are the M3 version with VVPAT capability, the older versions being M1 and M2. They are built and encoded with once-write software (read-only masked memory) at the state-owned and high-security

premises of the Bharat Electronics Limited and the Electronics Corporation of India Limited. The inventory of election EVMs is securely tracked by the Election Commission of India on a real-time basis with EVM Tracking Software (ETS). This system tracks its digital verification identity and physical presence. The M3 EVMs has embedded hardware and software that enables only a particular control unit to work with a particular voting unit issued by the Election Commission, as another layer of tamper-proofing. Additional means of tamper proofing the machines include several layers of seals. Indian EVMs are stand-alone non-networked machines.

## 3.4 Procedure to use

The control unit is with the presiding officer or a polling officer and the balloting Unit is placed inside the voting compartment. The balloting unit presents the voter with blue buttons (momentary switch) horizontally labelled with corresponding party symbol and candidate names. The Control Unit, on the other hand, provides the officer-in-charge with a "Ballot" marked button to proceed to the next voter, instead of issuing a ballot paper to them. This activates the ballot unit for a single vote from the next voter in the queue. The voter has to cast his vote by once pressing the blue button on the balloting unit against the candidate and symbol of his choice.

As soon as the last voter has voted, the Polling Officer-in-charge of the Control Unit will press the 'Close' Button. Thereafter, the EVM will not accept any votes. Further, after the close of the poll, the Balloting Unit is disconnected from the Control Unit and kept separately. Votes can be recorded only through the Balloting Unit. Again, the Presiding officer, at the close of the poll, will hand over to each polling agent present an account of votes recorded. At the time of counting of votes, the total will be tallied with this account and if there is any discrepancy, this will be pointed out by the Counting Agents. During the counting of votes, the results are displayed by pressing the 'Result' button.

There are two safeguards to prevent the 'Result' button from being pressed before the counting of votes officially begins. (a) This button cannot be pressed till the 'Close' button is pressed by the Polling Officer-in-charge at the end of the voting process in the polling booth. (b) This button is hidden and sealed; this can be broken only at the counting centre in the presence of a designated officer.

# CHAPTER-4

# Proposed Architecture

## 4.1 Introduction

The proposed digital EVM was designed using Verilog HDL the proposed method consists of several stages. In the first stage, the person should enter the unique code if it is matched, then flow proceeds to next stage. In this stage, we decide the total no. of voters and the total number of contestants taking part in the election process.

We have assigned Voting enable which is active high input signal for the voter in order to cast his vote by using voter switch input signal for making this election process more secure and safe. In the next stage, voting process begins when the voter casts his vote to a particular party or contestants the polled vote is registered in the individual contestant registry. In final stage, after completion of voting process the votes are validated by comparing the votes polled to the contestants with their registries after which the election process ends.

## 4.2 EVM Schematic

The EVM schematic is shown in below figure with four inputs and seven outputs. The Schematic of proposed electronic voting machine with input and output signals. The block diagram consists of clk, voting _enable, person and voter _switch as input signals. The dout, opled, party0, party1, party2, nota and invalid as output signals. Person is verified and then voting enable is input high and voter will vote by pressing the corresponding desired Party voters _switch, dout stores total valid votes and invalid votes are Discarded.

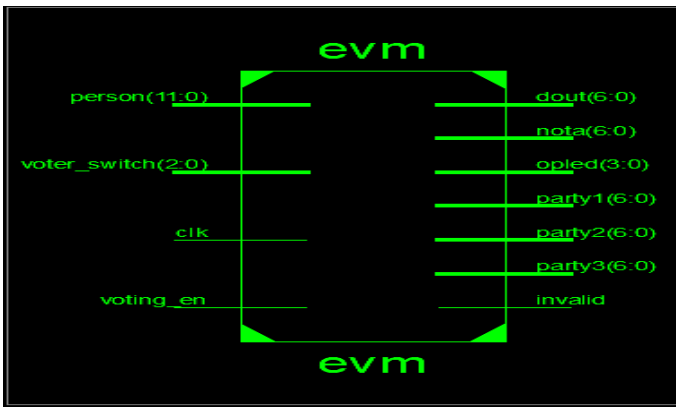


**FIGURE 6: EVM SCHEMATIC**

## 4.3 EVM Design and Implementation

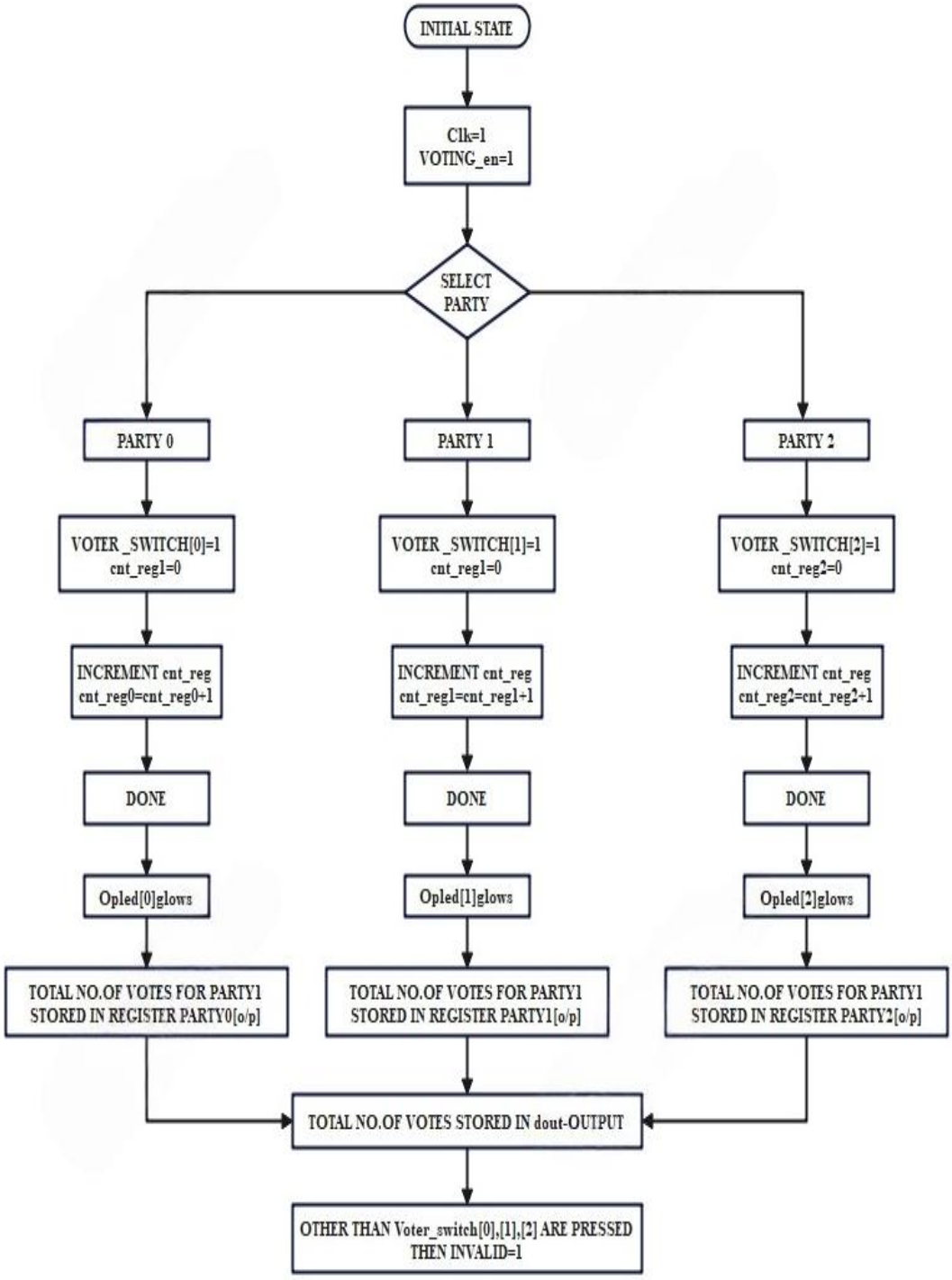


**FIGURE 7: FLOW CHART OF PROPOSED EVM**

## 4.4 Description of Signals used in Implementation

| S. No | Signal | Signal Type | Description |
|---|---|---|---|
| **1** | Clk | Input | Default clk is applied as input to the system |
| **2** | Voting _enable | Input | It is a active high signal which when enabled then the voting process begins |
| **3** | Voter _switch | Input | This signal determines the total no. of parties participating in the election process, in the present design it [3 down to 0] switch |
| **4** | person | Input | Person has unique id which needs to be verified. |
| **5** | Opled | Output | This signal is high when the corresponding voter switch is enabled which helps to identify whether the vote is registered to a corresponding party or not. |
| **6** | Party0 | Output | This register holds the total no. of votes polled to party0 |
| **7** | Party1 | Output | This register holds the total no. of votes polled to party1 |
| **8** | Party2 | Output | This register holds the total no. of votes polled to party2 |
| **9** | Nota | Output | This register holds the total no. of votes polled to Nota |
| **10** | Dout | Output | This register holds the total no. of votes polled in the entire election process of all the parties. |
| **11** | Invalid | Output | This signal is high whenever the invalid votes are polled. |

The proposed digital EVM was designed (fig2) using Verilog HDL and the proposed model consists of several stages. In the first stage, the person should enter the unique code if it is matched, then flow proceeds to next stage. In this stage, we decide the total no. of voters and the total number of contestants taking part in the election process.

We have assigned Voting enable which is active high input signal for the voter in order to cast his vote by using voter switch input signal for making this election process more secure and safe. In the next stage, voting process begins when the voter casts his vote to a particular party or contestants the polled vote is registered in the individual contestant registry.

In final stage, after completion of voting process the votes are validated by comparing the votes polled to the contestants with their registries after which the election process ends. The proposed electronic voting machine with input and output signals like clk, voting _enable, person and voter _switch which act as input signals. The dout, opled, party0, party1, party2, and invalid will act as output signals. The voting process in the first phase begins with the input clock signal (up to 100 MHz). At each positive edge of the clock signal the Voting _enable signal is synchronized. Voting _enable is a active high signal which when enabled then the voting process begins.

This signal plays a key role in election process because the vote casted by the voter is valid if and only if this Voting _enable signal is made high. So, this signal can be controlled by a polling officer at the polling booth. Voter _switch is another input signal used in our design. This signal determines the total no. of parties contesting in the election process, in the present design it [3 down to 0] switch. This signal allocates a switch to each party contesting in the election process. person is another input signal with unique code which needs to be entered and verified and if is matched then match signal is enabled In the proposed design we have taken three parties for contesting the election process.

At the point when the voter is prepared to make his choice the surveying official ought to confirm whether the clock, and voting _enable the two signals are high and unique code is verified if it is matched, then match signal is enabled and now the voter can cast his vote of his own choice by enabling the corresponding Voter _switch signal. Now, after casting the vote the output led of the corresponding party glows which indicate that his vote has been casted successfully. In the present design we have allocated three led's to three

parties who are contesting in the elections. So, whenever the clock signal is high and Voting _enable is high and say Voter _switch [0] is enabled the corresponding op led [0] glows. This process continues for the entire election process until the voting process concludes that is all the voters in that polling booth cast their votes to the parties of their choice. Now, once when the entire process completes, the dout register consists of the total no of valid votes polled in the election process. This helps in knowing the total votes polled. The party0, party1 and party2 registers will contain the votes polled to the corresponding parties individually in order to determine the winner.

# CHAPTER-5

# Software Requirements

## 5.1 Xilinx ISE

Xilinx, Inc. is the world's largest provider of programmable common-sense devices, the inventor of the field programmable gate array (FPGA) and the primary semiconductor organization with a fabless manufacturing version. Xilinx designs, develops and markets programmable logic merchandise including incorporated circuits (ICs), software program design equipment and predefined gadget functions added as intellectual property (IP) cores, design offerings, patron education, area engineering and technical assist. Xilinx sells each FPGAs and CPLDs programmable common-sense devices for electronic equipment producers in cease markets along with communications, commercial, customer, automobile and statistics processing.

Xilinx's FPGAs have even been used for the ALICE (A huge Ion Collider test) on the CERN ecu laboratory at the French-Swiss border to map and disentangle the trajectories of heaps of subatomic debris. The Vertex-II seasoned, Virtex-6, Virtex-5, and Virtex-6 FPGA families are mainly focused on gadget-on-chip (SOC) designers due to the fact they consist of up to two embedded IBM PowerPC cores. The ISE layout Suite is the critical digital design automation (EDA) product own family sold by using Xilinx. The ISE design Suite features include design access and synthesis assisting Verilog or VHDL, place-and-route (PAR), completed verification and debug using Chip Scope pro equipment, and advent of the bit documents which can be used to configure the chip. XST-Xilinx Synthesis era performs device particular synthesis for Cool Runner XPLA3/-II and XC9600/XL/XV households and generates an NGC report ready for the CPLD more fit.

## 5.2 Xilinx ISE 13.5

Xilinx is the maximum important tool and, in this device, we are able to carry out both simulation and synthesis.

### 5.2.1 Simulation

In this process, we are going to verify our required output to get the simulation technique first of all we need to enforce a top module (combination of all modules) after which in the simulation conduct, we can simulate the result

### 5.2.2 Synthesis

Synthesis process defines converting Verilog code into gate level which creates a net list.

### 5.2.3 Procedure

- Click project navigator
- Create new project
- Selection of FPGA

**Create new source**

- Select source type (Verilog module)
- Coding
- Declaration of inputs and output
- Sources for implementation

**Synthesize – XST**

- Check syntax
- View design summary
- View RTL schematic
- View technology schematic
- Sources for behavioural simulation

**Create new source**

- Select source type (Verilog text fixture)
- Write test bench code
- Xilinx ISE simulator

- Behavioural check syntax
- Simulate behavioural mode

## 5.3 Procedure for Synthesis

1. To create new project in Xilinx we should open the file menu, click on new project then it will open the dialog box as below in that type the filename click on next

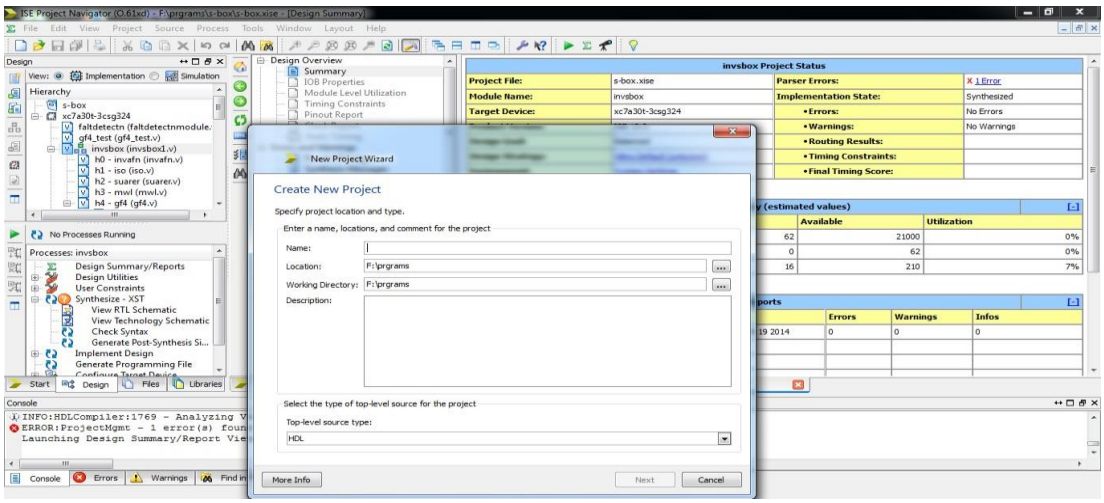


**FIGURE 8: CREATE NEW PROJECT IN XILINX**

2. Then it plays one more dialog box which will give us the specifications of the project, click on next

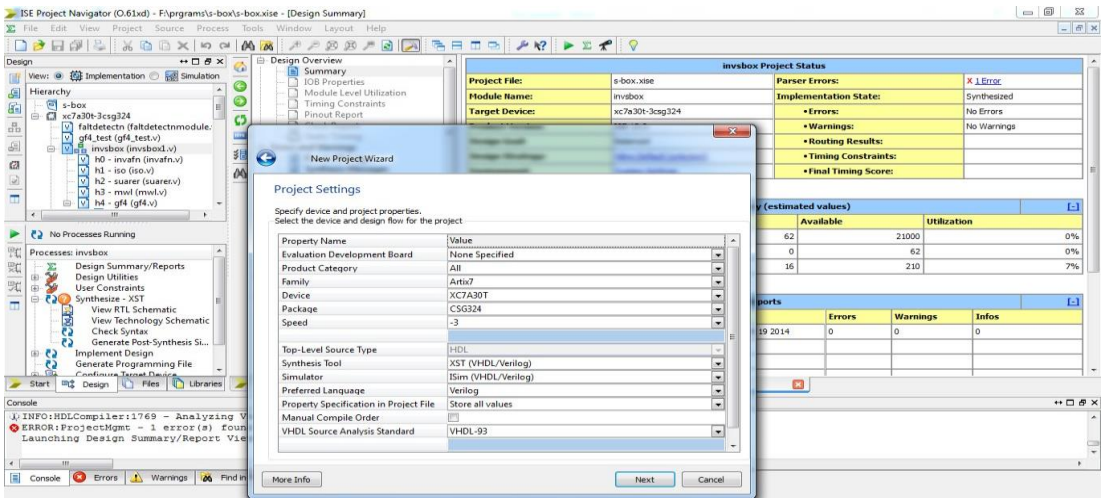


**FIGURE 9: GIVE SPECIFICATION OF THE PROJECT**

3. Then it again displays a dialog box as shown below with the created project description and click finish to complete the process of creating new project

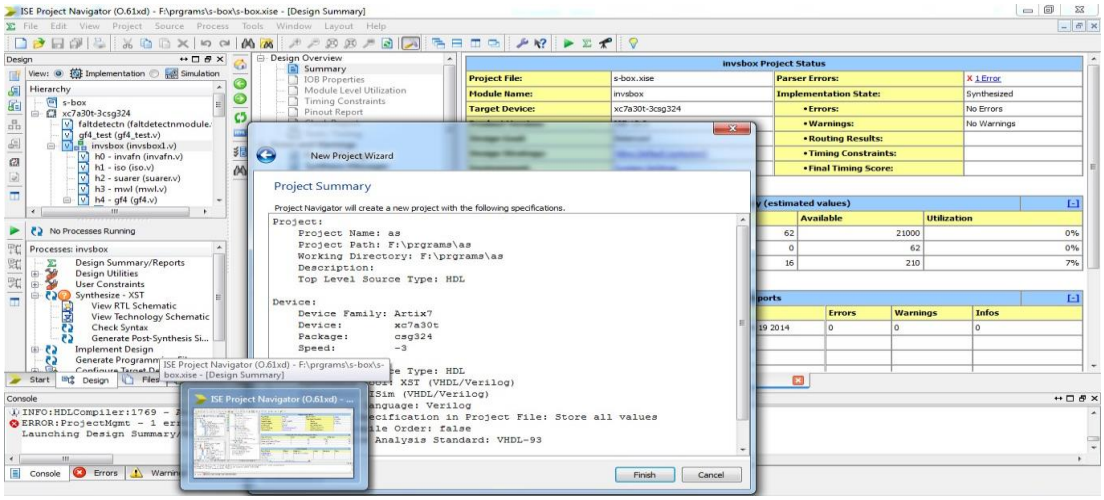


**FIGURE 10: CREATING NEW PROJECT COMPLETED**

4. Now project with specified name is created then create the Verilog files in the project. To create files, right click on the project that will show options like as shown below

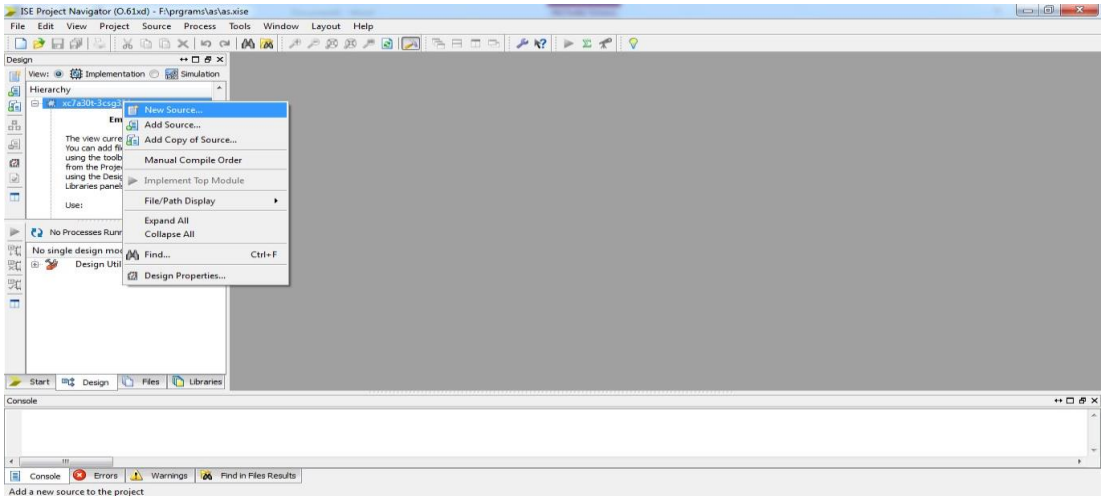


**FIGURE 11: CREATE A NEW SOURCE FILE**

5. From the given options select new source then it displays dialog box which is containing of list of file format now we want to create verilog file so select verilog module and give the name to the file. Then click on next

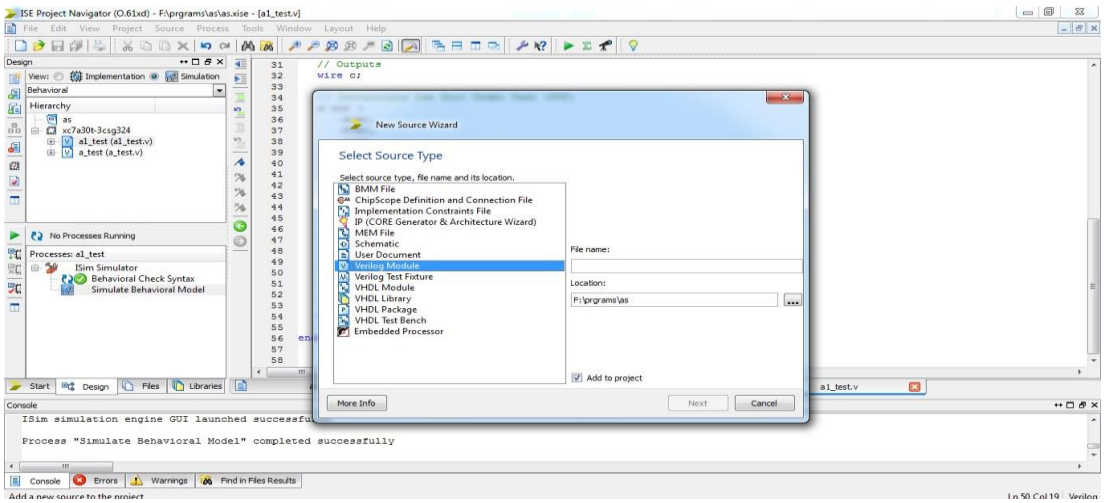


**FIGURE 12: AFTER CREATING NEW SOURCE FILE SELECT VERILOG MODULE**

6. Then it will ask us to select inputs and outputs. We can specify our inputs and outputs here else we may also specify as part of programme depend upon the user requirement, click on next

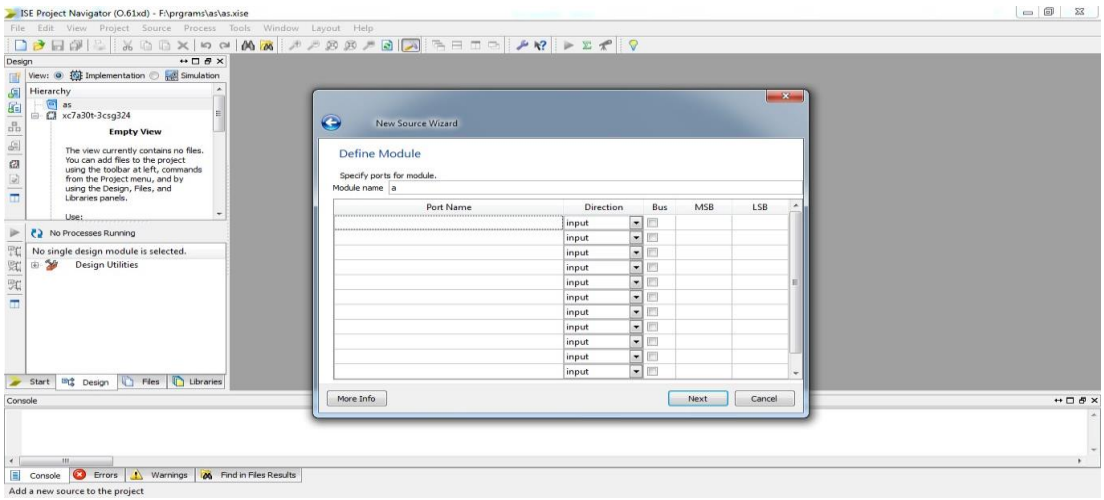


**FIGURE 13: SELECT INPUTS AND OUTPUTS**

7. It will again display a dialog box by giving details of filename etc, click on next

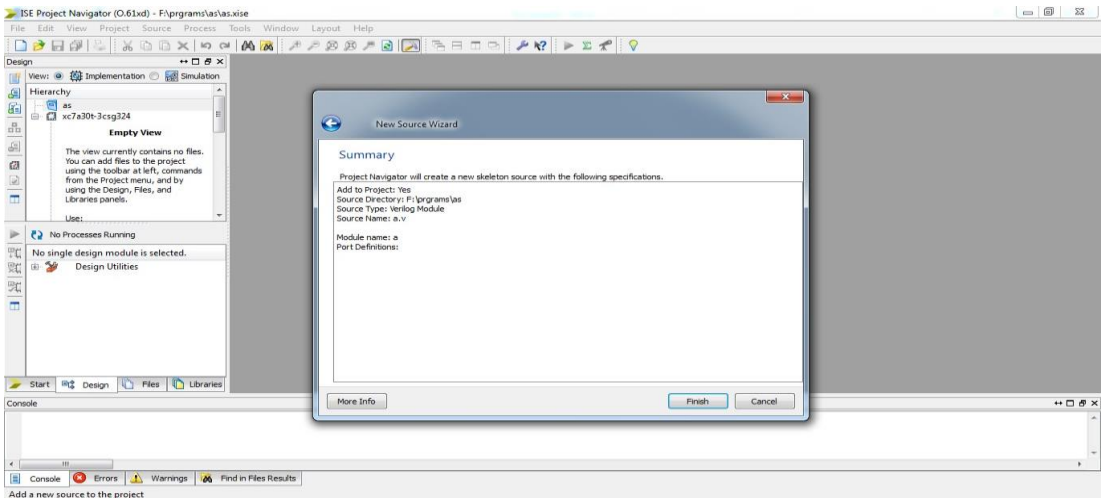


**FIGURE 14: DISPLAYS THE DETAILS OF THE FILE**

8. It will open a white space in the project window containing filename the double click on the file name so that it will displays respective file window, where we should write the code

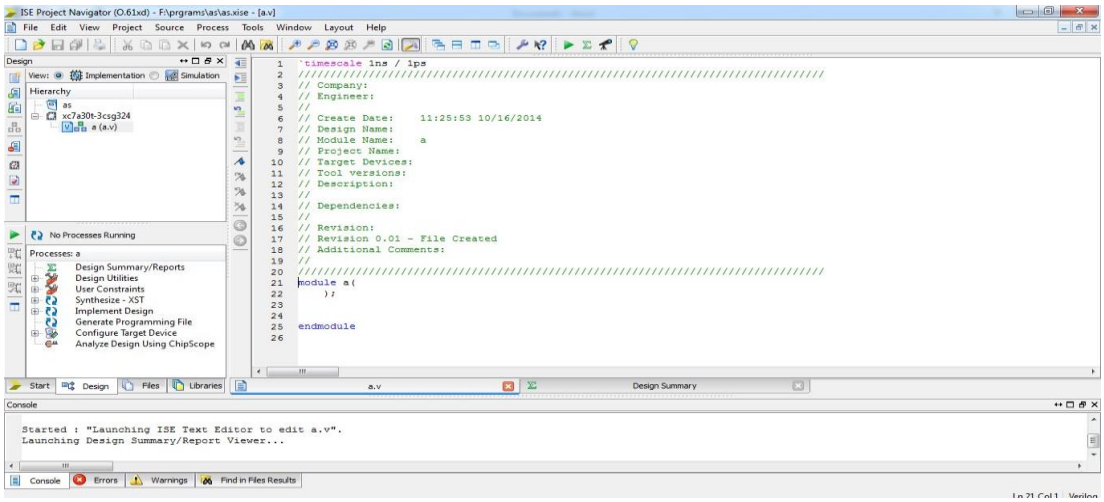


**FIGURE 15: WRITE THE CODE**

9. After completion writing code select the file name and click on synthesis which will check for errors, if there are any errors in syntax or design errors are checked and shown in the below of file window

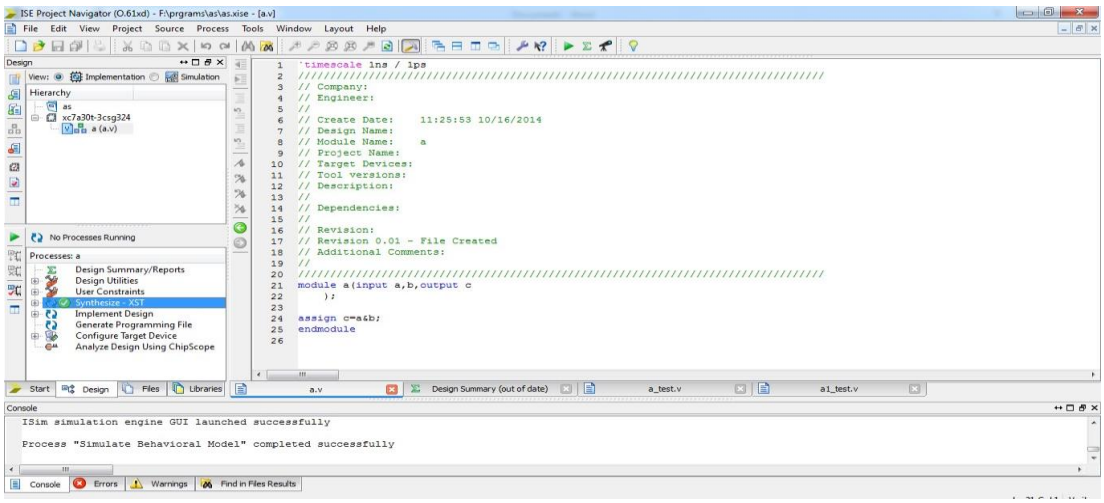


**FIGURE 16: SYNTHESIS THE CODE CHECK FOR ERRORS**

10. After successful synthesis we should have to create test bench file with extension as test, for that again right click on the file name as shown below, give filename

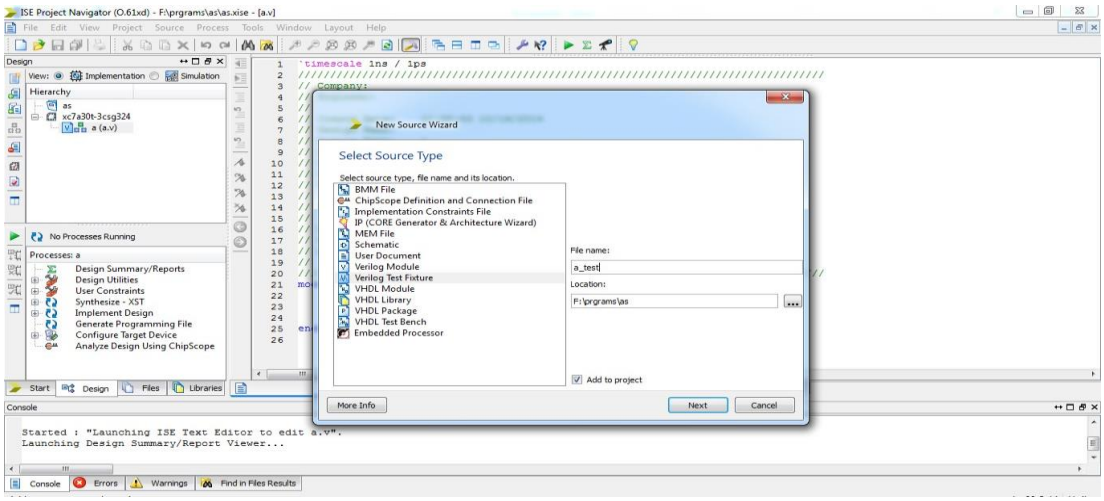


**FIGURE 17: CREATE NEW TEST BENCH**

11. If there are list files then select file for which we are creating the test bench. Click on next

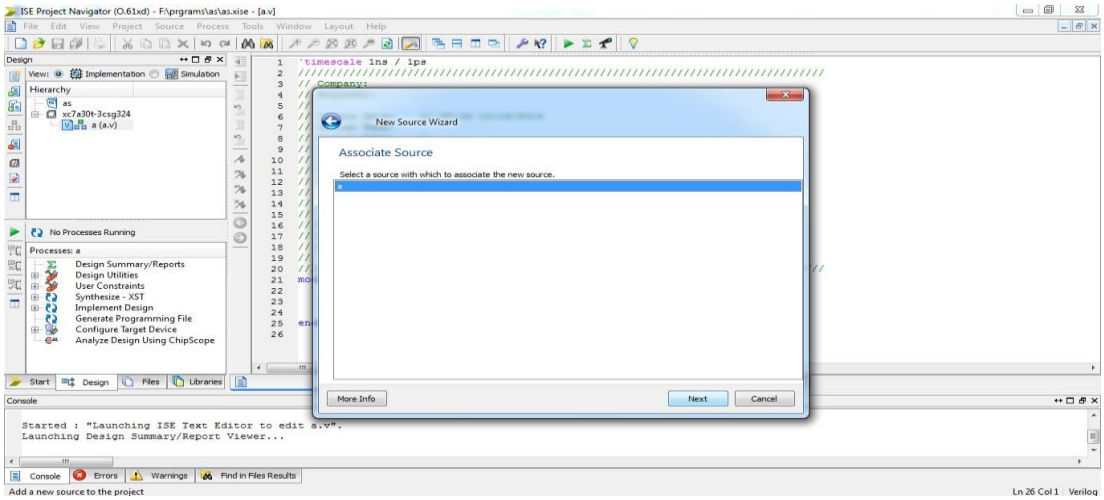


**FIGURE 18: CREATING TEST BENCH**

12. It again gives a testbench file in the project window, then give required inputs

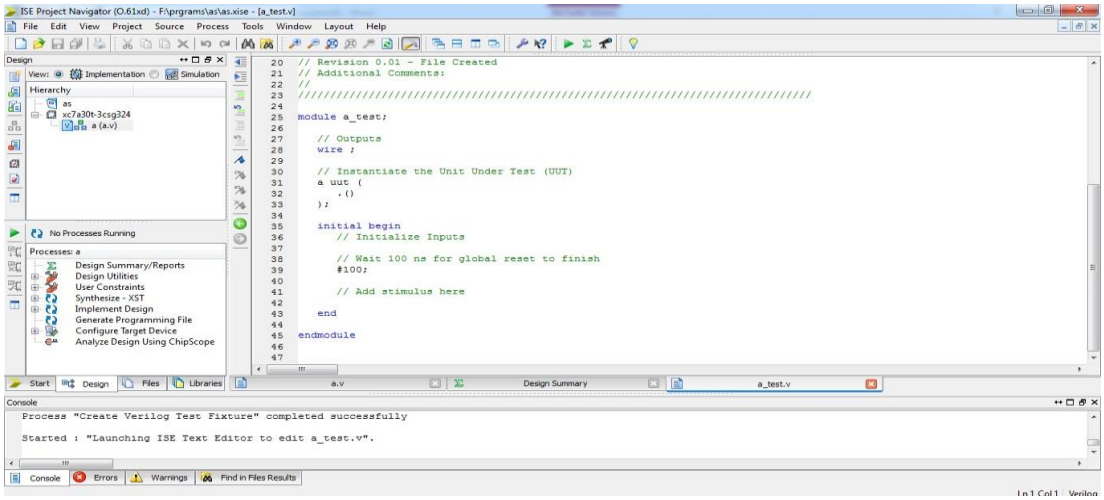


**FIGURE 19: WRITE TEST BENCH CODE**

13. select simulation from the view bar in the project window above the hierarchy window as follows.

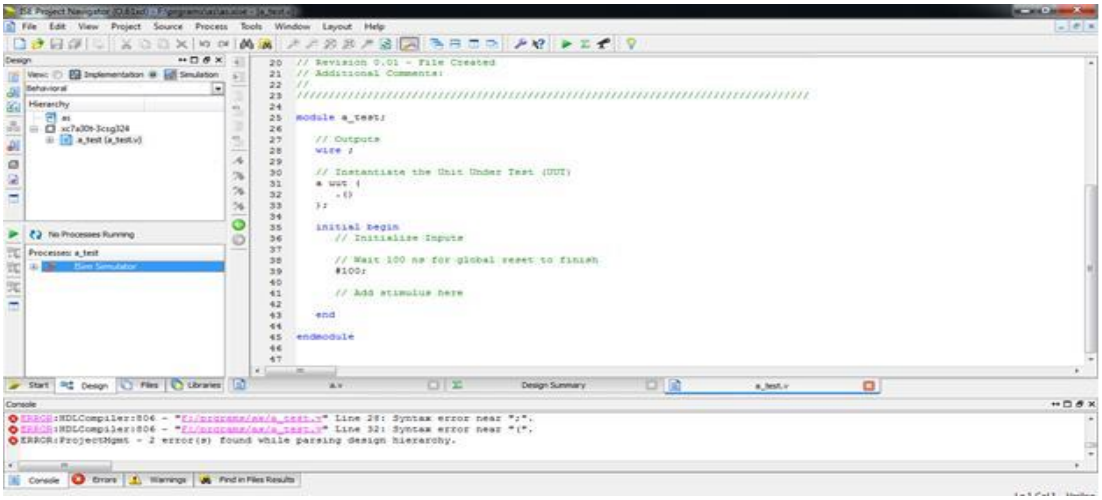

**FIGURE 20: RUN SIMULATION**

14. Double click on Isim Simulator it will expand as follows click on behavioural check syntax and it will check for syntax errors in test bench file.

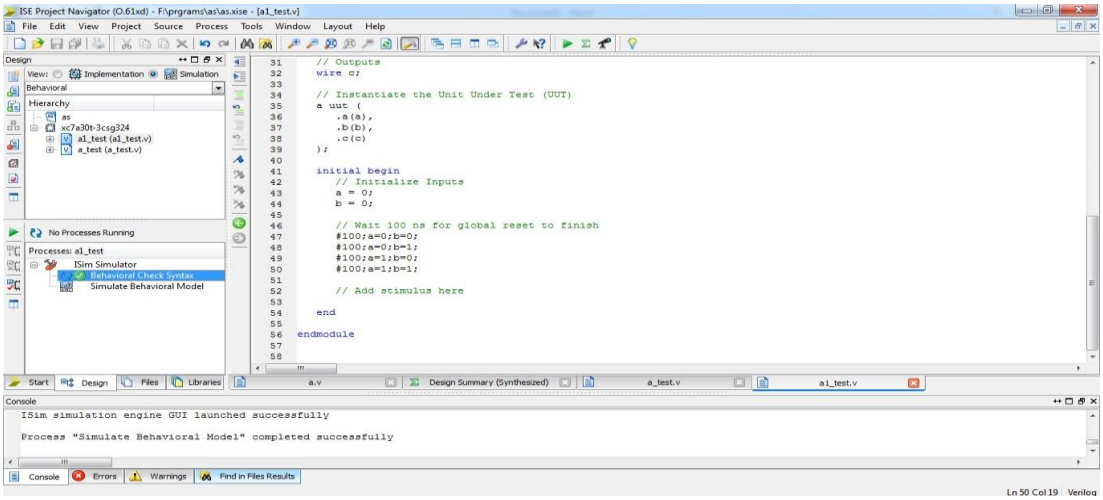


**FIGURE 21:BEHAVIORAL CHECK SYNTAX**

15. click on simulate behavioural model, it will display wave form for in response to the inputs given in the test bench file

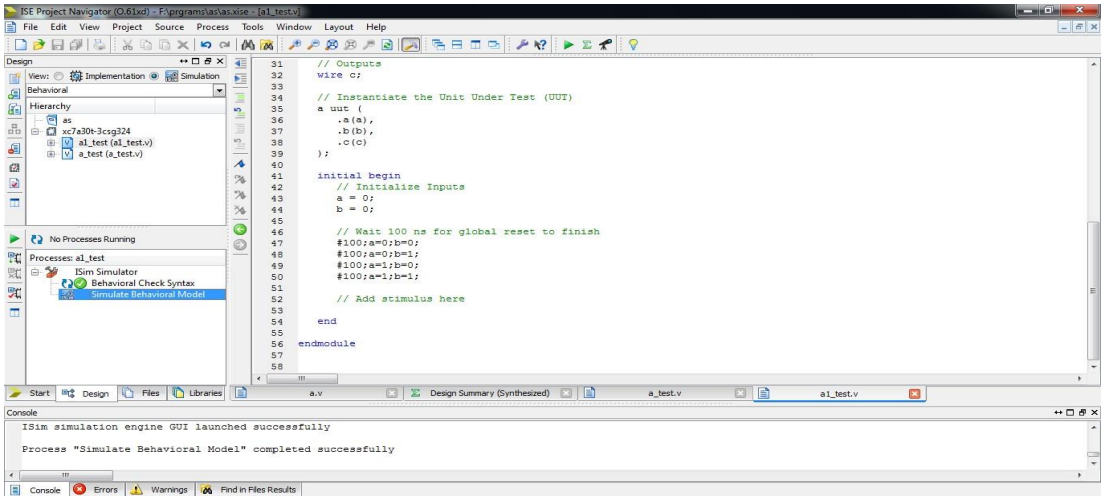


**FIGURE 22: SIMULATE BEHAVIORAL MODEL**

16. That wave form window having option to zoom out, zoom in to analyse the wave form clearly in order to understand behaviour of design

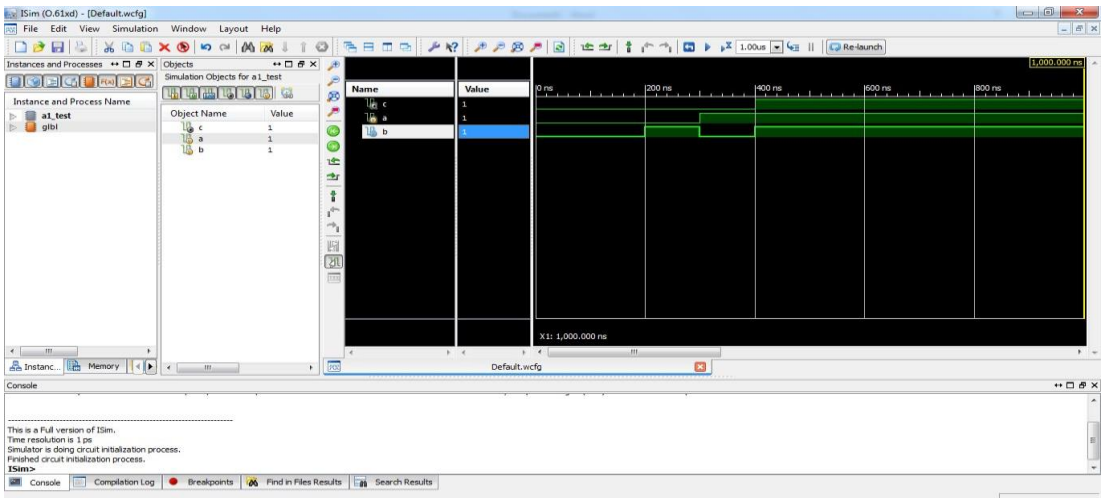


**FIGURE 23: OUTPUT OF THE DESIGN**

# CHAPTER:6

# Verilog HDL

Verilog is one amongst the chief regular Hardware Description Languages (HDL) utilized by PC circuit (IC) architects. HDL's licenses style to be recreated before inside the outline cycle in order to right mistakes or try different things with totally diverse models. Styles spoke to in lipoprotein zone unit innovation free, easy to style and redress, and range unit now and then a considerable measure of decipherable than schematics, fundamentally for enormous circuits. The Verilog is utilized to clarify the partner advanced rationale circuit is an interconnection of ports. The displaying strategies zone unit

- Basic (Structural),
- Behavioural,
- Dataflow.

## 6.1 Modeling Techniques

### 6.1.1 Data Stream

In this form we can depict the parts without a moment's delay by the connection among them. Module is a catchphrase which signifies the relationship between particular components within it. The module call is and entryway that is having data sources and yields are pronounced as in the bracket.

The dole out statement is a watchword which indicates plays out the operation particular. At that point it will spare the expense in the lefthand aspect operand. End module proclamation means that completing touch of module.

### 6.1.2 Behavioural

That is the demonstrating method that is utilized to characterize the element without knowing it. We can adaptation the behaviour. We can outline the issue by method for its conduct best. The dependably watchword recommends a free running technique. This proposes zero running test system. When an always obstruct achieved its given, it's far rescheduled (yet again). Parameters inside the Parenthesis are called affectability posting. The affectability list which recommends while information sources are assessed then constantly square can

be accomplished. The if else proclamation is comparable like as in C. while the separate affirmation is right comparing outcomes may be expert.

### 6.1.3 Structural Demonstrating

That is utilized to format an intricate module the utilization of straightforward sub module of it. The sub modules or the added substances which can be utilized routinely inside the bigger applications. These techniques will make complex applications yet basic design.

## 6.2 Modules

In Verilog, circuit added substances are planned inside a module. Modules can fuse both basic and behavioural explanations. Auxiliary proclamations constitute circuit segments like rationale doors, counters, and chip. Behavioural degree proclamations are customizing explanations that have no immediate mapping to circuit added substances like circles, if-then articulations, and jolt vectors which may be utilized to practice a circuit. Underneath code demonstrates an occurrence of a circuit and an investigate seat module. A module begins off developed with the watchword module joined by utilizing a non-mandatory module name and a non-necessary port rundown. The essential thing phrase end module closes a module.

## 6.3 Structural Design with Gate and Delay Operator

Verilog characterizes some essential practical insight entryways as a part of the dialect. Module some rationale part instantiates two door primitives: the not entryway and the AND entryway. The yield of the door is the primary parameter, and the information sources are whatever remains of the parameters. These primitives are versatile with the goal that you can get more than one information entryways basically by means of including contributions to the parameter posting.

## 6.4 Structural Design with Assignment Statements

On the off chance that you have many irregular great judgments; the door primitives of the previous segment are dreary to utilize in light of the fact that all the inner wires should be announced and set up viably. Every once in a while, it's miles less muddled to simply depict a circuit the use of an unmarried Boolean condition. In Verilog, Boolean conditions that have

practically identical planning houses as the door primitives are portrayed the use of a constant mission statement.

## 6.5 Structural Design with using Modules

Verilog helps progressive design by utilizing allowing modules to instantiate different modules. As a matter of course the planning inside a module is controlled through the module itself. However, modules can be characterized to have parameterized delays like the (6, five) put off administrator utilized with entryway primitives. In the module definition, utilize the parameter watchword to make puts off variables. Parameters additionally can be utilized to change other scalar qualities in the module. At the point when the module is instantiated then you could supersede the put off qualities utilizing the documentation.

## 6.6 Behavioural Design with Initial and always Blocks

Behavioural code is utilized to portray circuits at a more dynamic level then the basic level explanations we have concentrated on. All Behavioural code happens inside either an underlying square or in a generally piece. A module can contain various preparatory and continually pieces. These behavioural pieces consolidate explanations that oversee reenactment time, realities take the path of least resistance articulations (like assuming then and case proclamations), and closing off and non-blocking proclamations.

• A beginning piece executes when all through a reenactment. Preparatory pieces are for the most part used to instate variables and to clarify jolt waveforms which exercise which weight the reproduction.

• An ordinarily piece continually rehashes its execution for the span of a recreation. Consistently squares generally join behavioural code that models the genuine circuit operation.

All through a recreation each dependably and each preparatory square start to execute at time zero. Each piece executes at the same time with each auxiliary articulation and all the distinctive behavioural squares. The accompanying example shows a behavioural SRAM form. The underlying square units the memory cells to 0 at startup. The always square executes at whatever point there's a substitute on the compose oversee line, the chip pick

line, or the location transport. As a workout, propagation and glue this code into a Verilog document and compose a test seat to practicing the model.

## 6.7 Structural data types: WIRE AND REG

Verilog bolsters basic data sorts alluded to as nets which model equipment associations between circuit added substances. The two most regular auxiliary data sorts are wire and reg. The string nets act like genuine wires in circuits. The retype keep their qualities till some other expense is set on them, much the same as a check in equipment thing. The assertions for twine and enrol pointers are inside a module however open air any underlying or typically square. The preparatory condition of a register is x obscure, and the preparatory country of a twine is z. Ports: Modules speak with each other through ports, the cautions ordered in the parameter list at the highest point of the module. Ports can be of sort in, out, and in out. Right here are three oversimplified controls for coordinating the basic records kind to the sort of port.

## 6.8 Behavioural data types: Integer, Real, and Time

The sorts in whole number and genuine are helpful records sorts to apply for checking in behavioural code pieces. Those data sorts act like their counter parts in other programming dialects. on the off chance that you at some point or another arrangement to blend your behavioural code you then could likely need to abstain from utilizing these records sorts because of the reality they habitually combine huge circuits. The information kind time can safeguard a unique test system esteem known as reenactment time which is extricated from the gadget trademark $time. The time insights might be utilized to help you investigate your recreations.

## 6.9 Number Syntax

Numbers in Verilog are inside the accompanying arrangement the scale is always exact as a decimal reach. On the off chance that no is exact then the default length is no less than 32bits and can be expansive relying upon the gadget. legitimate base configurations are 'b , 'B , 'h , 'H 'd , 'D , 'o , 'O for twofold, hexadecimal, decimal, and octal. Numbers comprise of series of digits (0-9, A-F, a-f, x, X, z, Z). The X's mean obscure, and the Z's recommend unreasonable impedance If no base design is itemized the wide assortment is accepted to be a decimal amount.

## 6.10 Behavioural Design with Blocking and Non- Blocking Statements

There are 2 types of undertaking articulations: hindering the utilization of the = administrator and non-barricading the use of the <= administrator. Closing off assignments act like successive code proclamations and execute while they are known as. Non-blocking time table occasions to happen at a while inside what's to come. This will be troublesome because of the reality strains that show up after a non-closing off attestation execute at the equivalent time as the non-blocking statement.

## 6.11 Arrays, Vectors, and Memories

Verilog underpins three comparable measurements frameworks alluded to as Arrays, Vectors, and recollections. Clusters are utilized to save various things of the same sort. Vectors are utilized to symbolize multi-bit transports. What's more, memories are varieties of vectors which can be gotten too much like equipment recollections. Look at the accompanying case to choose an approach to reference and utilize the unprecedented actualities structures.

# CHAPTER-7

# Results

## 7.1Synthesis Results

### 7.1.1 RTL Schematic

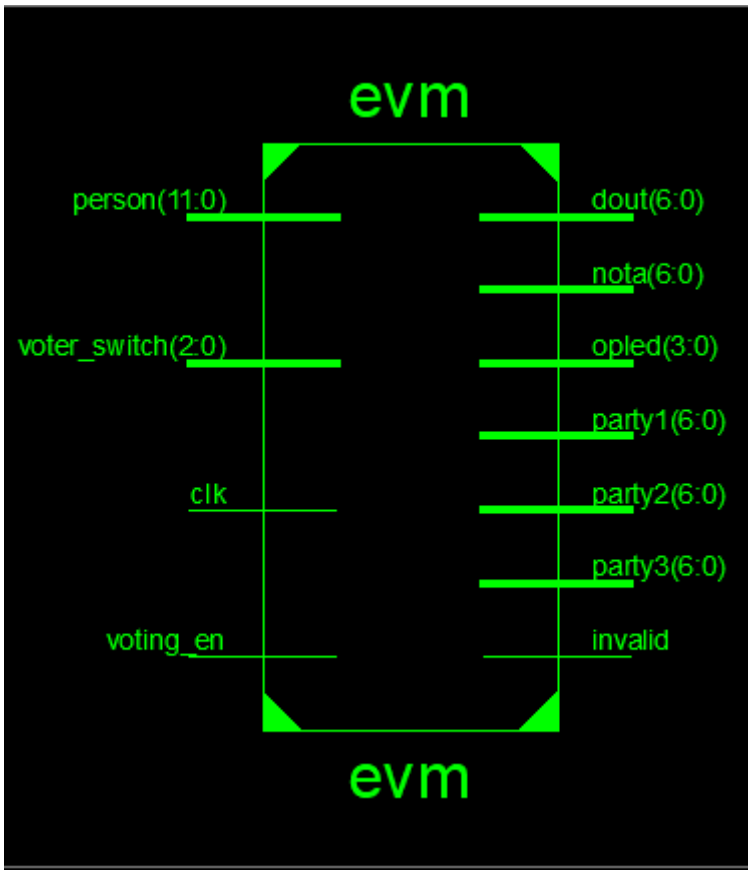


**FIGURE 24: RTL SCHEMATIC OF XILINX BASED EVM**

### 7.1.2 RTL Schematic(SYNTHESIS)

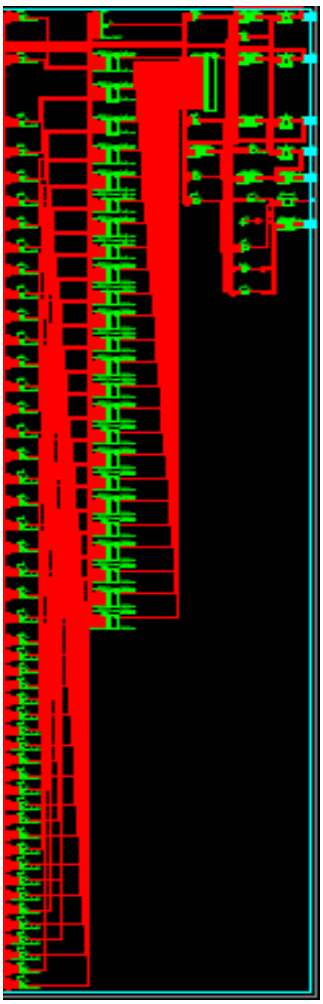

**FIGURE 25: INTERNAL RTL SCHEMATIC OF XILINX BASED EVM**

## 7.2 Simulation Result

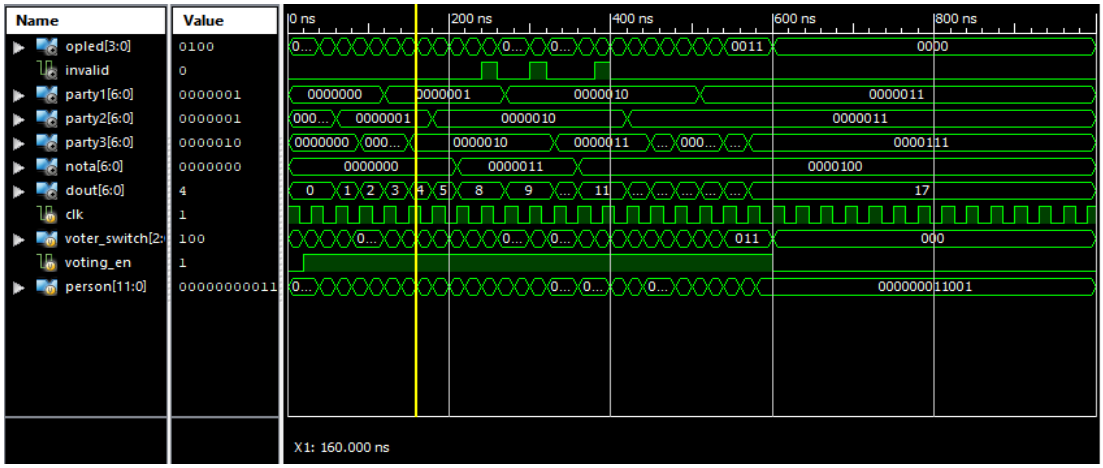


**FIGURE 26: SIMULATION RESULT 1**

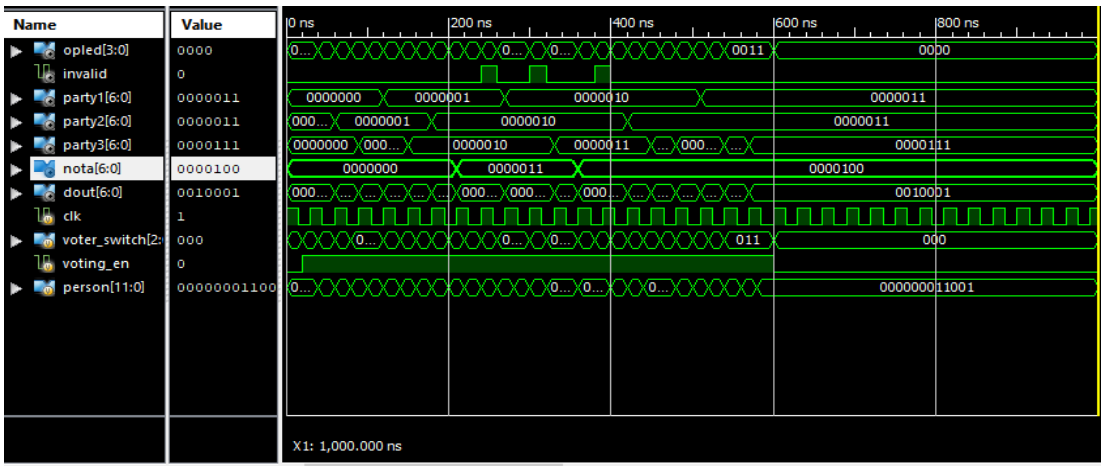


**FIGURE 27: SIMULATION RESULT 2**

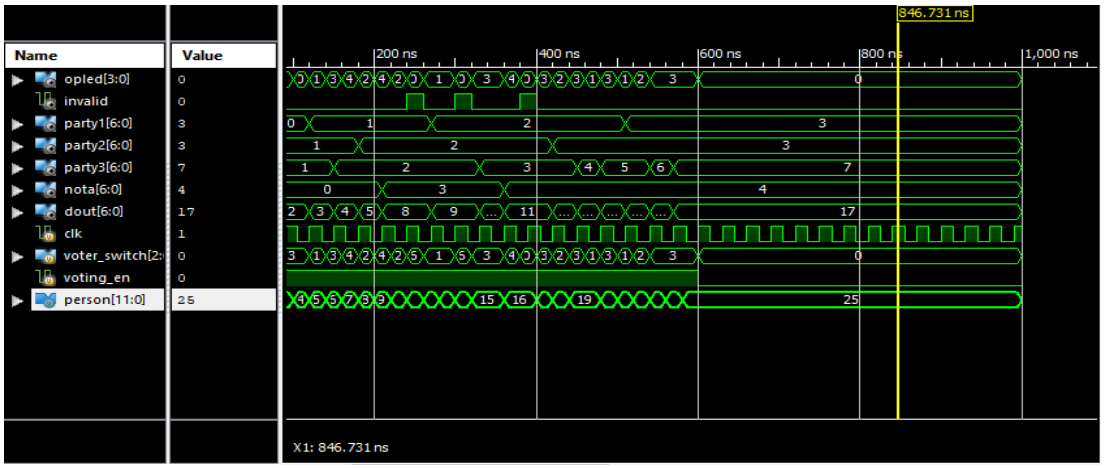


**FIGURE 28: SIMULATION RESULT 3**

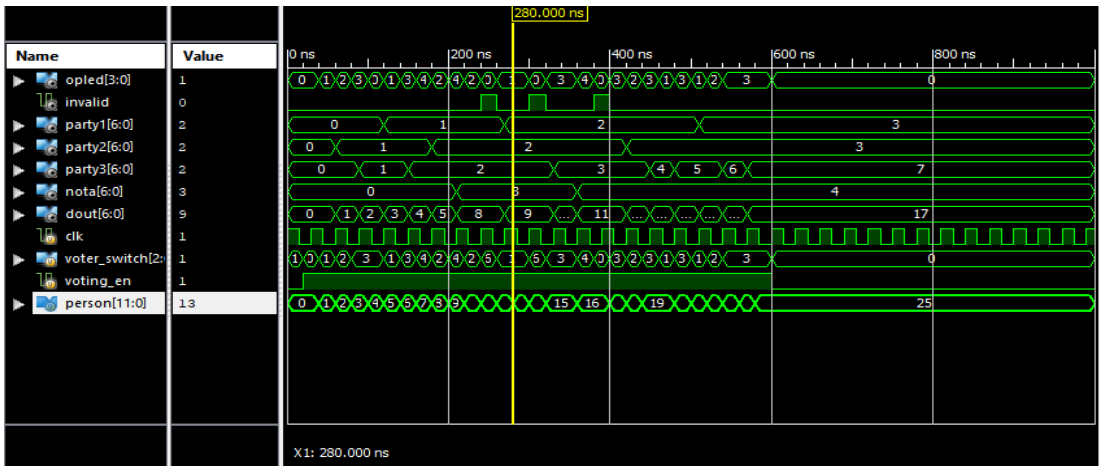


**FIGURE 29: SIMULATION RESULT 4**

## Advantages

- **Enhanced Security:** Ensures only eligible voters can vote through unique biometric identification.
- **Reliability:** Hardware design reduces risk of software errors or system failures.
- **Cost-Effective:** Optimized hardware use and customization lower costs.
- **Scalability:** Easily expandable to support large-scale elections and system integration.
- **Data Integrity:** Hardware-based storage makes tampering with data more difficult.
- **Real-Time Authentication:** Instant biometric verification ensures smooth voting.
- **Energy Efficiency:** Low power consumption ensures long operational life.
- **Transparency:** Hardware can be audited, making the process more trustworthy.

## Limitations

- **Privacy Concerns:** Biometric data could be misused or stolen if not properly secured.
- **Environmental Sensitivity:** Biometric sensors may be affected by environmental factors like lighting or dirty fingers.
- **System Dependency:** Reliance on hardware and software systems can make the process vulnerable to technical failures or cyberattacks.
- **Voter Accessibility:** Certain individuals (e.g., those with disabilities) may face difficulties using biometric systems.
- **False Rejections/Acceptances:** Biometric systems might fail to correctly authenticate some individuals, leading to false rejections or acceptances.
- **Cost of Implementation:** High initial costs for developing and deploying biometric-based machines.

## Conclusion

The Xilinx based EVM met the requirements of election process such as Enrolling the total no. of voters and contestants and allowing the voter to cast his vote to a particular party of his choice which in turn is confirmed by opled. In the final stage it compares all the validate votes polled to different parties and confirm the winner of the election. It mainly provides a special authentication process before voting process that increases the security and transparency.

## Future Scope

The proposed model with authentication with unique code and voter Id can bring new reforms in Election process, this can also be implemented for Aadhar authentication which can help us to highly transparent voting and truly elected people can be declared as the winner.

## References


1. Smith, T.F., Waterman, M.S.: Identification of Common Molecular Subsequence. J. Mol.Biol. 147, 95–197 (1981).
2. May, P., Ehrlich, H.C., Steinke, T.: ZIB Structure Prediction Pipeline: Composing a complex Biological Workflow through Web Services. In: Nagel, W.E., Walter, W.V., Lehner, W. (eds.) Euro-Par 2006. LNCS, vol. 4128, pp. 1148–1158. Springer, Heidelberg (2006).
3. Czajkowski, K., Fitzgerald, S., Foster, I., Kesselman, C.: Grid Information Services for Distributed Resource Sharing. In: 10th IEEE International Symposium on High Performance Distributed Computing, pp. 181–184. IEEE Press, New York (2001).
4. Foster, I., Kesselman, C., Nick, J. Tuecke, S.: The Physiology of the Grid: a Open Grid Services Architecture for Distributed Systems Integration. Technical report, Global Grid Forum (2002).
5. N.S.N. LAKSHMI PATHI RAJU, A. PRAVIN, N. S. MURTHY SHARMA, S. S. KIRAN A Novel Proposal on Implementation of Polling Percentage Improvement System Through Embedded Based Integration of Electronic Voting Machine and Other Methodologies – IJ ETA ETS ISSN: 0974-3588 | JULY ‟12 – DECEMBER ‟12 | Volume 5: Issue 2 pp 1-5.
6. Govindaraj, Ramya, and P. Kumaresan. "Online Voting System using Cloud." 2020 International Conference on Emerging Trends in Information Technology and Engineering (ic-ETITE). IEEE, 2020.
7. Bhattacharrya, Soma, et al. "Wireless voting machine." 2019 International Conference on Opto-Electronics and Applied Optics (Optronix). IEEE, 2019.
8. Bhuvana Priya, R., P. Sivapriya, and V. K. G. Kalaiselvi. "Smart voting." 2017 2nd International Conference on Computing and Communications Technologies (ICCCT). IEEE, 2017.
9. Abeesh A, Amal Prakash P, Arun R Pillai, Ashams H S, Dhanya M, Seena R, “Electronic Voting Machine
10. Authentication using Biometric Information”, NCETET - 2017 Conference Proceedings.
11. Sheela, AC Santha, and Ramya G. Franklin. "E-Voting System Using Homomorphic Encryption Technique." Journal of Physics: Conference Series. Vol. 1770. No. 1. IOP Publishing, 2021.